



Application Notice Title

Application Note for MOVX SRAM

Revision History

Rev.	History	Issue Date	Remark
1.0	Initial issue	December 13, 2004	Preliminary

PRELIMINARY

AP180 MEMORY ORGANIZATION

There are three distinct memory areas: scratchpad registers, program memory, and data memory. All registers and program memory are located on-chip but data memory spaces can be either on-chip, or off-chip.

The internal data memory is disabled after a power-on reset, and any MOVX instruction directs the data memory access to the external data memory. To enable the internal data memory, software must set the enable bit “ENINRAM” (RAMCON.0). On-chip data memory is provided by the 1KB SRAM and occupies addresses 0000h through 03FFh. MOVX operation for accessing external SRAM are through P0 and P2, and for internal SRAM are through internal separate address and data buses. If the internal data memory is enabled, the address bus A10~A15 are don't care and MOVX addresses greater than 003FFh will also access the internal 1KB memory depend on A9~A0 address bus.

The user can access data memory by the MOVX instructions with 16-bit (@DPTR) or 8-bit (@Ri) address. If it is with 8-bit address, the MSB addresses default from P2. An optional function is supported that the MSB addresses could be from the SFR register TP2 by setting the bit “EN-TP2” (CPUCTRL.0). At this situation, P2 can not be used for MSB addresses any more, but can be used for I/O port.

Figure1. MEMORY MAP

