



## High Performance 8-bit MCU

**AP180**  
**DATA SHEET**  
**December 2004**

### Document Title

High Performance 8-bit MCU

### Revision History

<u>Rev.</u>	<u>History</u>	<u>Issue Date</u>	<u>Remark</u>
1.0	Initial issue	April 27, 2004	Preliminary
1.1	SFR "ADC0CN" initial value: C1H => 40H SFR "DACON" initial value: C3H => C0H	July 12, 2004	Page 25 Page 28
1.2	Added preventing inadvertent Flash code programming description	October 21, 2004	Page 20
1.3	MOVX Data SRAM Description for P2/TP2 and internal 1K SRAM	December 15, 2004	Page 19
1.4	Operating voltage: 2.7V~3.6V => 3.0V ~ 3.6V	January 10, 2005	

PRELIMINARY

## GENERAL DESCRIPTION

The AP180 is a fully integrated, mixed-signal system IC. A conventional 8051 generates machine cycles using the clock frequency divided by 12. The AP180 offers the highest performance available in 8051-compatible microcontrollers. It features a redesigned processor core that executes every 8051 instruction (depending on the instruction type) up to 12 times faster than the original for the same crystal speed.

The AP180 supports standard resources such as three timer/counters, four 8-bit I/O ports, and a serial port. It provides several new hardware features implemented by new SFRs such as dual data pointers, a second serial port, an A/D converter, and two voltage output D/A converters. It also has on-chip JTAG interface and logic to support FLASH read and write operations, and non-intrusive in-circuit debug. The JTAG interface is implemented via four dedicated pins on the processor, which are TCK, TMS, TDI, and TDO.

## FEATURE

### HIGH SPEED RISC-BASED CPU CORE

- 1 clock-per-machine cycle.
- DC to 16MHz operation.
- Either MOVX or IO port to access fast/slow SRAM peripherals.
- Dual data pointers.
- Industry Standard 8051 compatible instruction set.
- Signed/Unsigned MUL AB instruction and Multiply Accumulator Function.

### MEMORY

- 256 bytes scratchpad RAM.
- Internal 1KB SRAM for MOVX.
- 64KB Flash Memory for ROM code, and 2 bits for security use.

### ON-CHIP DIGITAL PERIPHERALS

- Four byte wide bidirectional I/O Port; 5V input tolerant except P14 to P17.
- Two full-duplex serial ports.
- 3 General Purpose 16-Bit Timer counters.
- Programmable Watchdog Timer.
- 10 Interrupt sources with 2-level interrupt priority.
- Watch-Dog Timer Function.

### ELECTRICAL CHARACTERISTICS

- Operating Ranges : 3.0V ~ 3.6V
- External clock frequency: Up to 16MHz.
- Typical operating Current: 20mA@16MHz.
- Multiple Power Saving mode: IDLE and Power Down Modes.
- Temperature range: -25 to +85

### ANALOG PERIPHERALS

#### SAR ADC

- 10-bit Resolution
- Up to 100 kbps
- Up to 4 channel Input Multiplexer

#### DAC

- 10-bit Resolution
- Up to 100 kbps
- Up to 2 channel Output

### ON-CHIP JTAG DEBUG

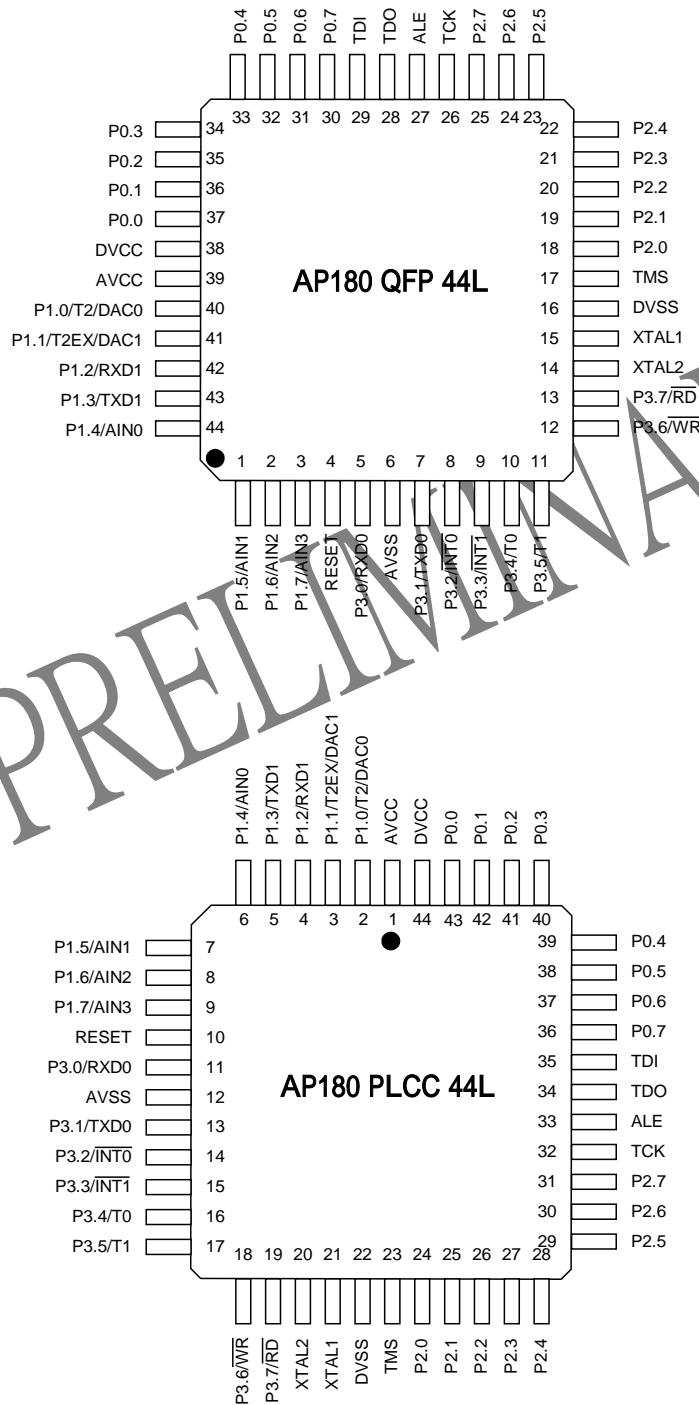
- 64KB/Security-Bits Flash memory In-System Programming through JTAG port (JTAG ISP).
- On-Chip Debug Circuitry facilitates non intrusive in-system debug (JTAG ICE).
- Provides two Breakpoints and Single-Step function.
- Inspect/Modify on-chip Memory and Registers.

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**Figure1. PIN CONFIGURATION**

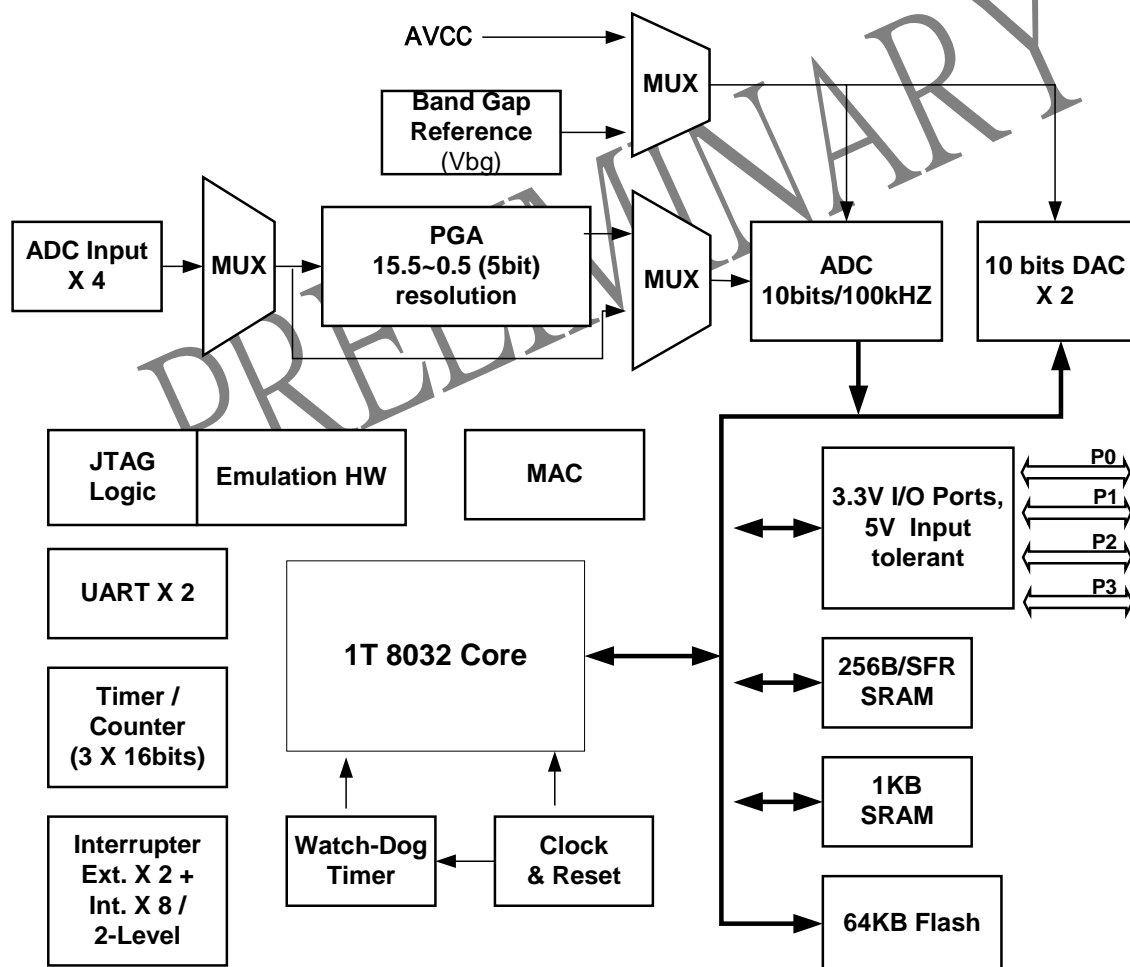


**Table1. ORDERING INFORMATION**

Part Number	Package Type	Operation Temperature Range
AP180-Q-I	Q = QFP	I = -25°C ~ +85°C
AP180-L-I	L = PLCC	

NOTE: CION Technology, Inc. reserves the right to make changes without prior notice.

### Figure2. BLOCK DIAGRAM



**Table2. PIN DESCRIPTIONS**

Signal name	PLCC Pin No.	QFP Pin No	Type	Signal Description
AVCC	1	39	A Pow	Analog Power Supply
P1.0/T2 / DAC0	2	40	I/O A Output	General I/O Port; Timer 2 External Count Input; DAC0 Output
P1.1/T2EX /DAC1	3	41	I/O A Output	General I/O Port; Timer 2 Capture/Reload Trigger; DAC1 Output
P1.2/RXD1	4	42	I/O	General I/O Port; Serial Port 1 Receive
P1.3/TXD1	5	43	I/O	General I/O Port; Serial Port 1 Transmit
P1.4/ Analog IN0	6	44	I/O A Input	General I/O Port; ADC Analog Input 0 (3.6V maximum input Only)
P1.5/ Analog IN1	7	1	I/O A Input	General I/O Port; ADC Analog Input 1 (3.6V maximum input Only)
P1.6/ Analog IN2	8	2	I/O A Input	General I/O Port; ADC Analog Input 2 (3.6V maximum input Only)
P1.7/ Analog IN3	9	3	I/O A Input	General I/O Port; ADC Analog Input 3 (3.6V maximum input Only)
RESET	10	4	Input	System External Reset Input
P3.0/RXD0	11	5	I/O	General I/O Port; Serial Port 0 Receive
AVSS	12	6	A Pow	Analog Power Ground
P3.1/TXD0	13	7	I/O	General I/O Port; Serial Port 0 Transmit
P3.2/ $\overline{\text{INT0}}$	14	8	I/O	General I/O Port; External Interrupt 0
P3.3/ $\overline{\text{INT1}}$	15	9	I/O	General I/O Port; External Interrupt 1
P3.4/T0	16	10	I/O	General I/O Port; Timer 0 External Input
P3.5/T1	17	11	I/O	General I/O Port; Timer1 External Input
P3.6/ $\overline{\text{WR}}$	18	12	I/O	General I/O Port; External Data Memory Write Strobe
P3.7/ $\overline{\text{RD}}$	19	13	I/O	General I/O Port; External Data Memory Read Strobe
XTAL2	20	14	Output	Crystal Oscillator Output
XTAL1	21	15	Input	Crystal Oscillator Input (3.6V maximum input Only)
DVSS	22	16	D Pow	Digital Power Ground
TMS	23	17	Input	Test Mode Select Input
P2.0	24	18	I/O	General I/O Port; External Data Memory A8



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Signal name	PLCC Pin No.	QFP Pin No	Type	Signal Description
P2.1	25	19	I/O	General I/O Port; External Data Memory A9
P2.2	26	20	I/O	General I/O Port; External Data Memory A10
P2.3	27	21	I/O	General I/O Port; External Data Memory A11
P2.4	28	22	I/O	General I/O Port; External Data Memory A12
P2.5	29	23	I/O	General I/O Port; External Data Memory A13
P2.6	30	24	I/O	General I/O Port; External Data Memory A14
P2.7	31	25	I/O	General I/O Port; External Data Memory A15
TCK	32	26	Input	Test Clock Input
ALE	33	27	Output	Address Latch Enable, default is at logic high
TDO	34	28	Output	Test Data Output
TDI	35	29	Input	Test Data Input
P0.7	36	30	I/O	General I/O Port; External Data Memory A7
P0.6	37	31	I/O	General I/O Port; External Data Memory A6
P0.5	38	32	I/O	General I/O Port; External Data Memory A5
P0.4	39	33	I/O	General I/O Port; External Data Memory A4
P0.3	40	34	I/O	General I/O Port; External Data Memory A3
P0.2	41	35	I/O	General I/O Port; External Data Memory A2
P0.1	42	36	I/O	General I/O Port; External Data Memory A1
P0.0	43	37	I/O	General I/O Port; External Data Memory A0
DVCC	44	38	D Pow	Digital Power Supply



### **AP180 DESCRIPTION**

The AP180 offers the highest performance available in 8051-compatible microcontrollers. A conventional 8051 generates machine cycles using the clock frequency divided by 12. In the AP180, the same machine cycle takes 1 clock. It features a redesigned processor core that executes every 8051 instruction (depending on the instruction type) up to 12 times faster than the original for the same crystal speed.

The AP180 instructions are 100% binary compatible with the industry standard 8051. All instructions perform the same function as their 8051 counterparts. Their effect on bits, flags, and other status functions is also identical. In general, software written for existing 8051-based systems works in the AP180 without any modification, with the exception of critical timing routines, since the AP180 performs its instructions much faster.

The AP180 is pin compatible with the same package of the standard 8051, but increases JTAG pins and analog power pins. It provides one 10-bit ADC, two 10-bit DACs for analog function and three 16-bit timer/counters, dual full-duplex serial ports, dual data pointers, Watchdog Timer, and 256 bytes of direct RAM plus 1kB of extra MOVX RAM. I/O ports can operate as in standard 8051 products. Timers default to a 12 clock-per-cycle operation to keep their timing compatible with original 8051 family systems. The dual data pointer feature also allows the user to eliminate wasted instructions when moving blocks of memory. The AP180 provides several new hardware features implemented by new SFRs.

### **SPECIAL FUNCTION REGISTERS (SFRs)**

All peripherals and operations that are not explicit instructions in the AP180 are controlled through SFRs. The most common features basic to the architecture are mapped to the SFRs. These include the CPU registers (ACC, B, PSW and MAC), data pointers (DPTRs), stack pointer, I/O ports, timer/counters, and serial ports. In many cases, an SFR controls an individual function or reports the function's status. SFRs whose addresses end in 0h or 8h are bit-addressable.

All standard SFR locations from the 8051 are duplicated in the AP180 and several SFRs have been added for the unique features of AP180. Most of these features are controlled by bits in SFRs located in unused locations in the 8051 SFR map. This allows for increased functionality while maintaining complete instruction set compatibility.



**Table3. SFR MEMORY MAP**

F8H	IP1							CPUCTRL	FFH
F0H	B		WDCON	RAMCON					F7H
E8H	IE1		DACON	DAC0L	DAC0H	DAC1L	DAC1H		EFH
E0H	ACC		ADC0H	ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH		E7H
D8H			ADC0CN	AMX0SL	ADC0PGA	ADC0CLK	ADC0SR	ADC0L	DFH
D0H	PSW								D7H
C8H	T2CON		RCAP2L	RCAP2H	TL2	TH2			CFH
C0H	SCON1	SBUF1	MAC0	MAC1	MAC2				C7H
B8H	IP								BFH
B0H	P3								B7H
A8H	IE								AFH
A0H	P2				TP2				A7H
98H	SCON	SBUF							9FH
90h	P1								97H
88H	TCON	TMOD	TL0	TL1	TH0	TH1			8FH
80H	P0	SP	DPL	DPH			DPS	PCON	87H

↑ Bit Addressable

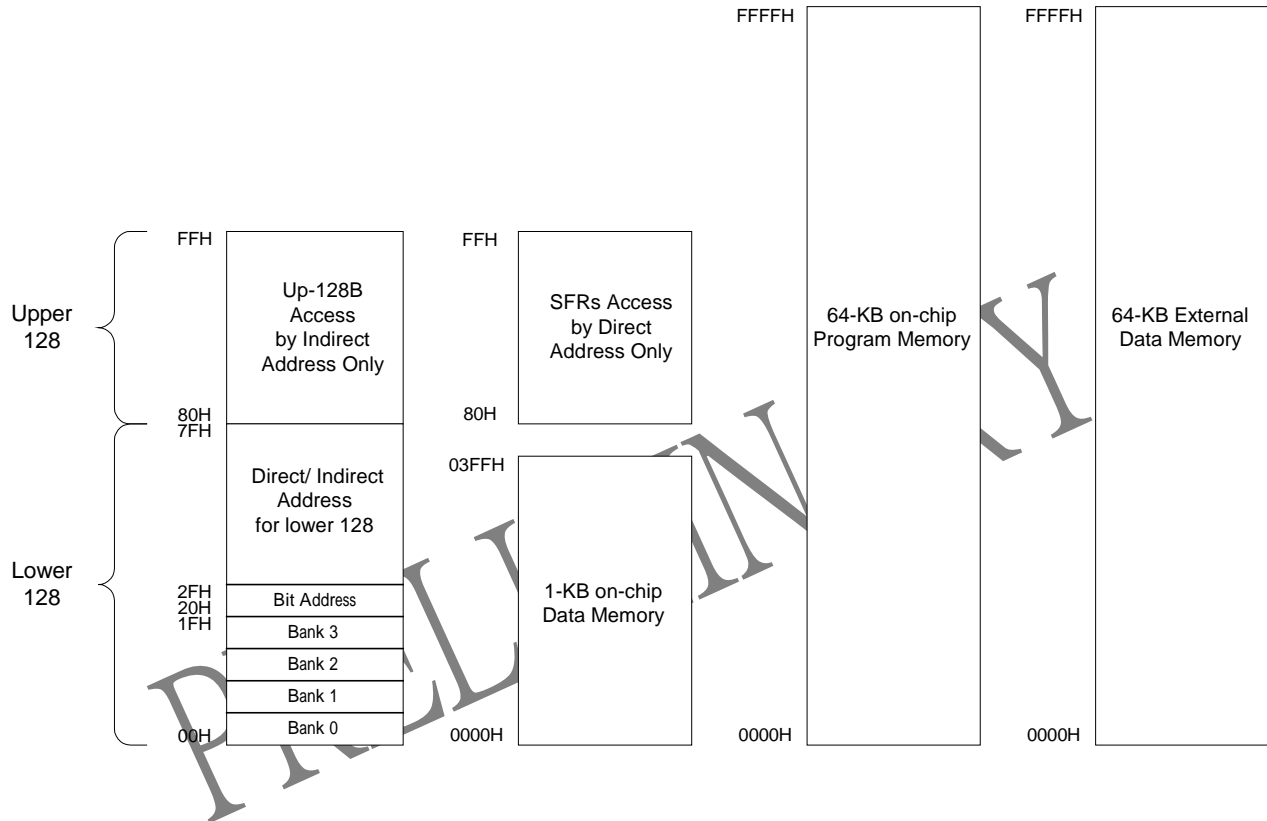
## MEMORY ORGANIZATION

There are three distinct memory areas in the AP180: scratchpad registers, program memory, and data memory. All registers and program memory are located on-chip but data memory spaces can be either on-chip, or off-chip. The AP180 incorporates two flash memory blocks for program memory, 64KB memory block is for main ROM code and 128B is for security use. For data memory, users can select either 1KB of on-chip or external data memory space up to 64KB.

Registers are located in the 256 bytes of on-chip RAM, which can be divided into two subareas of 128 bytes each. The upper 128 bytes are overlapped with the 128 bytes of SFRs in the memory map. The upper 128 bytes are accessed by indirect address, and the SFR area is accessed by direct address. The lower 128 bytes can be accessed by direct or indirect address.

There are four banks of eight individual working registers in the lower 128 bytes of scratchpad RAM which can be addressed by any instructions that use R0 to R7. In the registers 20h-2Fh are bit-addressable by software using Boolean operation instructions.

**Figure3. MEMORY MAP**



**Table4. SPECIAL FUNCTION REGISTERS SUMMARY**

REG	ADD	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Reset Value
P0	80H	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	#FFH
SP	81H	-	-	-	-	-	-	-	-	#07H
DPL	82H	-	-	-	-	-	-	-	-	#00H
DPH	83H	-	-	-	-	-	-	-	-	#00H
DPS	86H	-	-	-	-	-	-	-	SEL	#00H
PCON	87H	SMOD_0	SMOD_1	-	-	GF1	GF0	PD	IDL	#00H
TCON	88H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	#00H
TMOD	89H	GATE	C/ $\overline{T}$	M1	M0	GATE	C/ $\overline{T}$	M1	M0	#00H
TL0	8AH	-	-	-	-	-	-	-	-	#00H
TL1	8BH	-	-	-	-	-	-	-	-	#00H
TH0	8CH	-	-	-	-	-	-	-	-	#00H
TH1	8DH	-	-	-	-	-	-	-	-	#00H
P1	90H	P1.7/ AIN3	P1.6/ AIN2	P1.5/ AIN1	P1.4/ AIN0	P1.3/ TXD1	P1.2/ RXD1	P1.1/T2EX /DAC1	P1.0/T2 /DAC0	#FFH
SCON	98H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	#00H
SBUF	99H	-	-	-	-	-	-	-	-	#00H
P2	A0H	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	#FFH
TP2	A4H	-	-	-	-	-	-	-	-	#00H
IE	A8H	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	#00H
P3	B0H	P3.7/ $\overline{RD}$	P3.6/ $\overline{WR}$	P3.5/ T1	P3.4/ T0	P3.3/ $\overline{INT1}$	P3.2/ $\overline{INT0}$	P3.1/ TXD0	P3.0/ RXD0	#FFH
IP	B8H	-	PS1	PT2	PS0	PT1	PX1	PT0	PX0	#00H
SCON1	C0H	SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	#00H
SBUF1	C1H	-	-	-	-	-	-	-	-	#00H
MAC0	C2H	-	-	-	-	-	-	-	-	#00H
MAC1	C3H	-	-	-	-	-	-	-	-	#00H
MAC2	C4H	-	-	-	-	-	-	-	-	#00H
T2CON	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/ $\overline{T2}$	CP/ $\overline{RL2}$	#00H
RCAP2L	CAH	-	-	-	-	-	-	-	-	#00H
RCAP2H	CBH	-	-	-	-	-	-	-	-	#00H
TL2	CCH	-	-	-	-	-	-	-	-	#00H
TH2	CDH	-	-	-	-	-	-	-	-	#00H

REG	ADD	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Reset Value
PSW	D0H	CY	AC	F0	RS1	RS0	OV	-	P	#00H
ADC0CN	DAH	-	ADCPWD	ADCTYP	ADCTM	ADCBUSY	ADCIF	ADWIF	ADCRJST	#40H
AMX0SL	DBH	-	-	PINSL1	PINSL0	AIN3EN	AIN2EN	AIN1EN	AIN0EN	#00H
ADC0PGA	DCH	-	-	PGAEN	AMPGN4	AMPGN3	AMPGN2	AMPGN1	AMPGN0	#00H
ADC0CLK	DDH	-	-	ADCD5	ADCD4	ADCD3	ADCD2	ADCD1	ADCD0	#00H
ADC0SR	DEH	ADSR7	ADSR6	ADSR5	ADSR4	ADSR3	ADSR2	ADSR1	ADSR0	#00H
ADC0L	DFH	-	-	-	-	-	-	-	-	#00H
ACC	E0H	-	-	-	-	-	-	-	-	#00H
ADC0H	E2H	-	-	-	-	-	-	-	-	#00H
ADC0GTL	E3H	-	-	-	-	-	-	-	-	#FFH
ADC0GTH	E4H	-	-	-	-	-	-	-	-	#FFH
ADC0LTL	E5H	-	-	-	-	-	-	-	-	#00H
ADC0LTH	E6H	-	-	-	-	-	-	-	-	#00H
IE1	E8H	-	-	-	-	-	EWDI	EADWI	EADCI	#00H
DACON	EAH	DAC1PWD	DAC0PWD	DAC1OE	DAC0OE	DAC1TYP	DAC0TYP	DAC1RJST	DAC0RJST	#C0H
DAC0L	EBH	-	-	-	-	-	-	-	-	#00H
DAC0H	ECH	-	-	-	-	-	-	-	-	#00H
DAC1L	EDH	-	-	-	-	-	-	-	-	#00H
DAC1H	EEH	-	-	-	-	-	-	-	-	#00H
B	F0H	-	-	-	-	-	-	-	-	#00H
WDCON	F2H	WDEN	WD1	WD0	-	EWT	RWT	WDIF	WTRF	#00H
RAMCON	F3H	-	-	-	-	-	SETALE	ALEOFF	ENINRAM	#00H
IP1	F8H	-	-	-	-	-	PWDI	PADWI	PADCI	#00H
CPUCTRL	FFH	-	-	-	-	-	-	EN-SIGN	EN-TP2	#00H

Note: Do not write 1 to un-used bit, it needs to keep the initial value.

## **FUNCTION DESCRIPTION**

### **INSTRUCTION SET**

The instruction set of the AP180 is fully compatible with the industry standard 8051. Standard 8051 development tools can be used to develop software for the AP180. All AP180 instructions are the binary and functional equivalent of 8051 counterparts, including opcodes, addressing modes and effect on PSW flags. However, instruction timing is much faster than that of the standard 8051 since AP180's machine cycles is with 1 system-clock length.

The AP180 provides a function with decrement for the data pointer by the instruction "DB A5H". Full detail of the instruction set summary is given in the application note AN-0001.

### **STACK POINTERS**

The stack pointer denotes the register location at the top of the stack, which is the last-used value. The user can place the stack anywhere in the scratchpad RAM by setting the stack pointer to the desired location, although the lower bytes are normally used for working registers. The Stack Pointer is initialized to 07H after a reset. This causes the stack to begin at location 08H.

### **I/O PORTS**

The AP180 offers four 8-bit I/O ports. Each I/O port is represented by an SFR location, and can be written or read. The I/O port has a latch that contains the value written by software. P0 to P3 are the SFR latches of Ports 0 to 3, respectively. The I/O port P0 to P3 are all with internal pull-high circuit.

### **ACCUMULATOR (A) & B REGISTER (B)**

ACC is the Accumulator register. The mnemonics for accumulator-specific instructions, however, refer to the accumulator simply as A. The B register is used during multiply and divide operations. For other instructions it can be treated as another scratchpad register.

## MULTIPLIER ACCUMULATOR (MAC)

An on-chip math accelerator allows the AP180 to perform 8 and 8-bit multiplier accumulator using dedicated hardware. MAC math operation is performed by the instruction “**MUL AB**” without any additional delay. The execution time of multiplier and multiplier accumulator is two clocks. Each time the MAC operation, the result is transparently added to a 24-bit accumulator. This can greatly increase speed of DSP and high-level math operations.

In the industry standard 8051, multiplication for register A and B is un-signed operation. The AP180 provides sign and un-signed operations by setting the bit “**EN-SIGN**”(CPUCTRL.1).

**Figure 4. MAC and CPUCTRL Register**

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								0000 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address
								MAC0: C2h
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								0000 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address
								MAC1: C3h
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								0000 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address
								MAC2: C4h
MAC: Multiplier Accumulator only operation with instruction “ <b>MUL AB</b> ”. $MAC = MAC + (A*B)$								
R	R	R	R	R	R	R/W	R/W	Reset Value
-	-	-	-	-	-	EN-SIGN	EN-TP2	0000 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address
								CPUCTRL: FFh
EN-SIGN: Default value is 0 that multiplier and MAC are un_sign ALU. If set it to 1, the multiplier and MAC are sign ALU.								
Bit 7-2: Reserved for future use.								

## COUNTER/TIMERS

Three 16-bit timer/counters are available in the AP180. Each timer is contained in two SFR locations that can be read or written by software. All three timers can be used as either counters of external events, where 1-to-0 transitions on a port pin are monitored and counted, or timers that increase content by 1 with every 12 system clocks. If Timer 2 is used as a baud rate generator, its time base is fixed at divide by 2, regardless of the setting of its timer mode bits.

Timers 0 and 1 both have three modes of operations. They can each be used as a 13-bit timer/counter, a 16-bit timer/counter, or an 8-bit timer/counter with auto-reload. Timer0 has a fourth operating mode as two 8-bit timer/counters without auto-reload. Each timer can also be used as a counter of external pulses on the corresponding T0/T1 pin for 1-to-0 transitions. The mode of operation is controlled by the timer mode (TMOD). Register pairs (TH0, TL0), and (TH1, TL1) are the 16-bit Counter registers for Timer/Counters 0 and 1 respectively. Timers 0 and 1 are enabled by the timer control (TCON) register.

Register pairs (TH2, TL2) are the 16-bit Counter registers for Timer/Counters 2. The register pair (RCAP2H, RCAP2L) are the Capture registers for the Timer 2 Capture Mode. In this mode, in response to a transition at the AP180's T2EX pin, TH2 and TL2 are copied into RCAP2H and RCAP2L. Timer 2 also has a 16-bit auto-reload mode, and RCAP2H and RCAP2L hold the reload value for this mode. Timer 2 is enabled by the T2CON register, and its mode of operation is selected by the T2MOD register.

## DATA POINTERS

The data pointer DPTR is used to assign a memory address for the MOVX instructions. This address can point to a MOVX RAM locating (on-chip or off-chip). There are two data pointers, the user can select the active pointer through a dedicated SFR bit "SEL" (DPS.0). If set logic 0 to "SEL", DPTR0 is active for use, and set logic 1 to "SEL", DPTR1 is active for use. To increase data pointer is by using instruction "INC DPTR", and to decrease it is by instruction "DB A5H".

## SERIAL PORTS

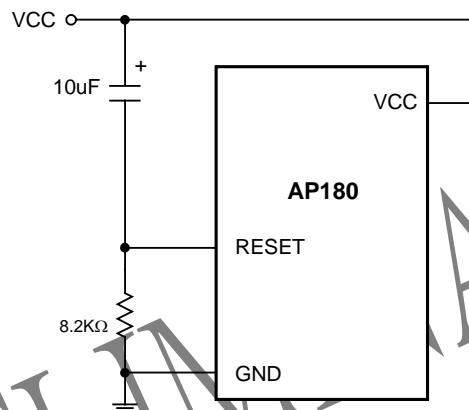
The AP180 provides dual serial ports (UARTs) that are controlled and accessed by SFRs. Each UART has an address that is used to read and write the UART. It provides a UART that is identical to the 80C52. In addition, it includes a second hardware UART that is a full duplicate of the standard one. This port optionally uses pins P12 (RXD1) and P13 (TXD1) and has duplicate control functions included in new SFR locations.

Each UART is controlled by its own SFR control register. Both ports can operate simultaneously but can be at different baud rates or even in different modes. The second serial port has similar control registers (SCON1 at C0h, SBUF1 at C1h) as the original. The new serial port can only use Timer 1 for timer-generated baud rates. The original serial port can use Timer 1 or Timer 2 or both for timer-generated baud rates.

## POWER-ON RESET

An automatic reset can be obtained when VCC goes through a 10 $\mu$ F capacitor and GND through an 8.2K resistor. The start-up time of internal MCU clock needs 32,768 clock cycles. This power-on reset circuit is shown in Figure 5. When power is turned on, the circuit holds the RESET pin high for an amount of time that depends on the value of the capacitor and the rate at which it charges.

Note that the port pins will be in a random state until the oscillator has start and the internal reset algorithm has written 1s to them.



**Figure 5. Power-on Reset Circuit**

## POWER-SAVING MODE OF OPERATION

The AP180 has two power-saving modes: Idle and Power-down mode. In the Idle mode (IDL = 1), the CPU is frozen. In Power-down mode (PD = 1), the whole IC is frozen.

### IDLE MODE

Idle mode suspends the processor by holding the program counter in a static state. No instructions are fetched and no processing occurs. The processor status is preserved in its entirety: the stack pointer, program counter, program status word, accumulator, and all other registers maintain their data during idle mode. The port pins hold the logical states they had at the time Idle was activated. Setting the bit “IDL”( PCON.0) to logic 1 invokes idle mode. The instruction that executes this step is the last instruction prior to freezing the program counter.

In the Idle mode, all peripheral clocks remain active, and the timers, watchdog, and serial ports functions continue to operate, so that the processor can exit the idle mode using any interrupt sources that are enabled. The IDL bit is cleared automatically once idle mode is exited. On returning from the interrupt vector using the RETI instruction, the next address



is the one that immediately follows the instruction that invoked the idle mode. Any processor resets also remove the idle mode. Since the clock oscillator is active, the reset must be held active for at least 2 oscillator cycles to complete the reset.

## **POWER-DOWN MODE**

The power-down mode disables all circuits within the processor. All on-chip clocks, timers, and serial port communication are stopped, and no processing is possible. Setting the bit “PD” (PCON.1) to logic 1 invokes power-down mode. The processor can exit power-down mode by using any of the external interrupts ( $\overline{\text{INT0}}$  or  $\overline{\text{INT1}}$ ). The external interrupt allows both the SFRs and the on-chip RAM to retain their values. The pulse width of low-level trigger signal needs to keep low at least 32768 clock cycles for waking up CPU from power-down mode.

An external reset by the RST pin unconditionally exits the processor from power-down mode. It redefines all special function registers but does not change on-chip RAM. When the power-down mode is removed, the processor waits for 32,768 clock cycles for the crystal to be stable before starting normal execution.

## **INTERRUPTS**

The AP180 provides 10 interrupt vector sources. All interrupts are controlled by a series combination of individual enable bits and a global enable bit “EA” (IE.7). Setting “EA” bit to logic 1 allows individual interrupts to be enabled. Setting it to logic 0 disables all interrupts regardless of the individual interrupt enable settings.

There are two levels of interrupt priority. All interrupts have individual priority bit in the interrupt priority registers to allow each interrupt to be assigned a priority level for high/low priority. All interrupts also have a natural hierarchy. In this manner, when a set of interrupts has been assigned the same priority, a second hierarchy determines which interrupt is allowed to take precedence. The natural hierarchy is determined by analyzing potential interrupts in a sequential manner with the order listed in Table5.

**Table5. INTERRUPT SUMMARY**

INTERRUPT	VECTOR	NATURE ORDER	FLAG	ENABLE	PRIORITY CONTROL
External Interrupt 0	03h	0	IE0 (TCON.1) **	EX0 (IE.0)	PX0 (IP.0)
Timer 0	0Bh	1	TF0 (TCON.5) *	ET0 (IE.1)	PT0 (IP.1)
External Interrupt 1	13h	2	IE1 (TCON.3) **	EX1 (IE.2)	PX1 (IP.2)
Timer 1	1Bh	3	TF1 (TCON.7) *	ET1 (IE.3)	PT1 (IP.3)
Serial Port 0	23h	4	RI (SCON.0) TI (SCON.1)	ES0 (IE.4)	PS0 (IP.4)
Timer 2	2Bh	5	TF2 (T2CON.7) EXF2 (T2CON.6)	ET2 (IE.5)	PT2 (IP.5)
Serial Port 1	33h	6	RI_1 (SCON1.0) TI_1 (SCON1.1)	ES1 (IE.6)	PS1 (IP.6)
ADC Interrupt	3Bh	7	ADCF (ADC0CN.2)	EADCI (IE1.0)	PADCI (IP1.0)
ADW Interrupt	43h	8	ADWIF (ADC0CN.1)	EADWI (IE1.1)	PADWI (IP1.1)
Watchdog Interrupt	4Bh	9	WDIF (WDCON.1)	EWDI (IE1.2)	PWDI (IP1.2)

\* Timer 0/1 interrupt flag is cleared automatically by hardware when the service routine is vectored to.

\*\* If the interrupt (INT0/INT1) is edge triggered, the flag is cleared automatically by hardware when the service routine is vectored to. If the interrupt is level triggered, the flag follows the state of the pin.

## MOVX DATA MEMORY

The user can use internal 1KB SRAM or external SRAM up to 64KB for data memory by setting the enable bit “ENINRAM” (RAMCON.0). The internal data memory is disabled after a power-on reset, and any MOVX instruction directs the data memory access to the external data memory. To enable the internal data memory, software must set the enable bit “ENINRAM”. On-chip data memory is provided by the 1KB SRAM and occupies addresses 0000h through 03FFh. MOVX operation for accessing external SRAM are through P0 and P2, and for internal SRAM are through internal separate address and data buses. If the internal data memory is enabled, the address bus A10~A15 are don't care and MOVX addresses greater than 003FFh will also access the internal 1KB memory depend on A9~A0 address bus.

The user can access data memory by the MOVX instructions with 16-bit (@DPTR) or 8-bit (@Ri) address. If it is with 8-bit address, the MSB addresses default from P2. An optional function is supported that the MSB addresses could be from the SFR register TP2 by setting the bit “EN-TP2” (CPUCTRL.0). At this situation, P2 can not be used for MSB addresses any more, but can be used for I/O port.

There are two data pointers in the AP180. After power-on reset, DPTR0 is default active. To select DPTR1 being active, software must set the bit “SEL” (DPS.0) to logic 1. To access data memory with instruction MOVX, the LSB address latch signal “ALE” is automatically toggled. AP180 supports user to stop the “ALE” signal by setting the bit “ALEOFF”, even supports user to self define the external data memory control signals through I/O ports for slow SRAM.

**Figure 6. DPS, RAMCON and CPUCTRL Register**

R	R	R	R	R	R	R	R/W	Reset Value
-	-	-	-	-	-	-	SEL	0000 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address
								DPS: 86h
SEL: Set 1/0 to select for DPTR1/DPTR. Bit 7-1: Reserved for future use.								
R	R	R	R	R	R/W	R/W	R/W	Reset Value
-	-	-	-	-	SETALE	ALEOFF	ENINRAM	0000 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address
								RAMCON: F3h
ENINRAM: Set 1/0 to enable/disable Internal 1KB (0000H~03FFH) Data memory. ALEOFF: Set1/0 to disable/enable ALE toggling during an MOVX memory access. (EMI Suppression) SETALE: Set1/0 for high/low output of ALE. Bit 7-3: Reserved for future use.								
R	R	R	R	R	R	R/W	R/W	Reset Value
-	-	-	-	-	-	EN-SIGN	EN-TP2	0000 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address
								CPUCTRL: FFh
EN-TP2: If EN-TP2 is 0, to access data memory by MOVX instruction with 8-bit addressing (@Ri), the MSB address is from register P2. If set EN-TP2, the MSB address is from register TP2. Bit 7-2: Reserved for future use.								

## ON-CHIP FLASH MEMORY

The AP180 has 64KB for on-chip main memory, and 128 bytes for security function. The full on-chip program memory size for main ROM code is 64KB which can be fetched by the processor automatically. The reset routines and all interrupt vectors are located in the individual addresses of the on-chip program memory area. The 128B for security function only one byte addressed 0000h called lock-bit is used, the others of 128B are unused.

The AP180 supports any of two programming methods. Serial programming is supported through the JTAG port and parallel programming is provided on the programmer. The AP180 will be set into parallel programming mode with Reset pin at logic high and P35 at logic low. The user must make sure that Pin P35 is not at logic low during high reset pulse, to prevent any inadvertent program or erase operations within the flash ROM code.

Full details of the parallel programming and JTAG ISP are given in the application note AN-0002 and AN-0003.

## SECURITY FEATURES

The AP180 supports three-level lock restricts viewing of the internal 64KB ROM code memory contents. By programming the two Lock-bit, the user can select a level of security as specified in Table6. Once a security level is selected and programmed, the setting of the Lock-bit remains. Only a mass erase can erase both 64KB and 128 bytes flash to allow reprogramming the security level to a less restricted protection.

## FLASH MEMORY LOCK-BIT

-	-	-	-	-	-	LB2	LB1	0000H
---	---	---	---	---	---	-----	-----	-------

**Table6. LOCK BITS FEATURES**

Level	LB2	LB1	Protection Type
1	U	U	No program lock feature enabled.
2	U	P	Data verification is disabled. ("Verify Lock Bits" is still enabled.)
3	P	P	Same as 2, also further written operation of the Flash is disabled.

Notes :

1. 'U' = Non programmed or "1" level.
2. 'P' = Programmed or "0" level

## JTAG

The AP180 has an on-chip JTAG interface to support FLASH read/write operations (JTAG ISP) and debug logic (JTAG ICE) that provide non-intrusive, in-circuit debug through the four-pin JTAG interface.

The ISP facility has made in-circuit programming in an embedded application possible with a minimum of additional expense in components and circuit board area. Only a small connector needs to order to use this feature. The AP180's debug system supports inspection and modification of SFR, internal 256B scratchpad RAM, on-chip 1KB SRAM and ROM memory. No additional target RAM, program memory, or communications channel are required. JTAG ICE function for break condition includes two break points and single step break. JTAG ICE does not support Watchdog Timer and power saving function. Before into JTAG mode, make sure IC is not in power saving mode or not enable Watchdog Timer.

The AP180DK is a development kit with all the hardware and software necessary to develop application code and perform in-circuit debug for the AP180. The Kit includes software with a developer's studio and debugger, an integrated 8051 assembler/Keil C, and an RS-232 to JTAG interface module referred to as the emulation cartridge. An RS-232 is the interface to PC, and JTAG port is the interface to target application board with an AP180 installed. The JTAG interface is implemented via four dedicated pins on the processor, which are TCK, TMS, TDI, and TDO. These pins are all 5 volt tolerant.

**Table7. JTAG PIN DESCRIPTION**

Pin Name	Pin Description
<b>TDI</b>	<b>Test Data Input</b> -This input provides a serial data stream to the JTAG. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.(50K ohm) Data is always shifted LSB-first.
<b>TDO</b>	<b>Test Data Output</b> -This tri-state output provides a serial data stream from the JTAG. It is driven in the Shift-IR and Shift-DR controller states of the JTAG state machine and changes on the falling edge of TCK.
<b>TCK</b>	<b>Test Clock Input</b> -This input proves a gate clock to synchronize the test logic and shift serial data through the JTAG port. The TCK pin has an on-chip pull-down resistor. (50K ohm)
<b>TMS</b>	<b>Test Mode Select Input</b> -This input sequences the TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. (50K ohm)

## WATCHDOG TIMER

The watchdog timer (WDT) is the source of both the watchdog interrupt and the watchdog reset. The WDT will force the processor into the interrupt and reset state when its function is enabled and the WDT overflows. The WDT reset and interrupt overflow are measured by counting system clock cycles. To prevent overflow, the WDT must be restarted by software set before the overflow occurs. If the system experiences a software/hardware malfunction preventing the software from restarting the WDT, it will overflow and cause a interrupt or reset. This should prevent the system from running out of control.

A watchdog control register (WDCON) is used for programming the functions. The WDT subsystem is enabled only when the bit “WDEN” is set to logic 1. The “EWT” is the enable bit for the watchdog timer reset function and the “RWT” is the bit used to restart the watchdog timer. Setting the RWT bit restarts the timer for another full interval. The “WDIF” is the interrupt flag set at timer termination and the “WTRF” is the reset flag set following a watchdog reset overflow. The WDT interrupt is enabled by the bit “EWDI” (IE1.2) when it is set to logic 1.

The WDT interrupt timeout has a default divide ratio of  $2^{17}$  of the crystal oscillator clock, with the watchdog reset set to timeout 512 system clock cycles later. The watchdog reset will occur only when hardware WDT overflows. Using the bits “WD0” and “WD1” in the control register, other divide ratios can be selected for longer watchdog interrupt periods.

**Figure 7. WDCON: Watchdog Control Register**

R/W	R/W	R/W	R	R/W	R/W	R/W	R	Reset Value
WDEN	WD1	WD0	-	EWT	RWT	WDIF	WTRF	0000 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address WDCON: F2h

WDEN: Watchdog Timer Enable Bit.  
 1: Watchdog Timer is Enabled. Watchdog is active.  
 0: Watchdog Timer is Disabled. (default)

WD1-0: Watchdog Timeout Value.  
 00:  $2^{17}$  clks for WDT interrupt timeout; ( $2^{17} + 512$  clks) for WDT Reset timeout.  
 01:  $2^{20}$  clks for WDT interrupt timeout; ( $2^{20} + 512$  clks) for WDT Reset timeout.  
 10:  $2^{23}$  clks for WDT interrupt timeout; ( $2^{23} + 512$  clks) for WDT Reset timeout.  
 11:  $2^{26}$  clks for WDT interrupt timeout; ( $2^{26} + 512$  clks) for WDT Reset timeout.

EWT: Set 0/1 to Disable/Enable Watchdog Timer Reset.

RWT: Set 1 to restart the Watchdog Timer for another full interval. RWT is cleared by hardware.

WDIF: Watchdog Timer Interrupt Flag. (Cleared by software)

WTRF: Reset Flag which is hardware set following a Watchdog reset timeout.  
 Set it to 1 if RESET is from Watchdog Timer timeout reset.  
 Clear it to 0 if RESET is not from Watchdog Timer timeout reset.

Bit 4: Reserved for future use.

## ANALOG FUNCTION

The AP180 incorporates analog peripheral functions: an analog to digital converter (ADC), dual digital to analog converter (DAC). Suggesting the user needs to support Analog power to IC whenever the analog function is used or not.

### 10-BIT ADC

The ADC subsystem for the AP180 consists of configurable analog multiplexer (AMUX), a programmable gain amplifier (PGA), and a 100ksps, 10-bit successive-approximation-register ADC and programmable window detector. The AMUX, PGA, Data Conversion Modes, and Window Detector are all configurable under software control via the SFRs. The ADC's voltage reference can be the analog power supply (AVCC), or Band-Gap voltage reference (Vbg) depending on the bits "ADCTYP". The ADC is in low power shutdown when the bit "ADCPWD" is set to logic 1.

### AMUX and PGA

The pins P14 to P17 may be selected via software for the analog input. The AMX0SL SFR is used to select the desired analog input pin. The PGA amplifies the input signal by an amount determined by the states of the AMPGN4-0 bits in the ADC programmable amplify register, ADC0PGA. The PGA can be software-programmed for gains of 0.5 to 15.5. The PGA default is disabled and the analog input directly connects to 10-bit SAR ADC input. (Bypass the PGA block default)

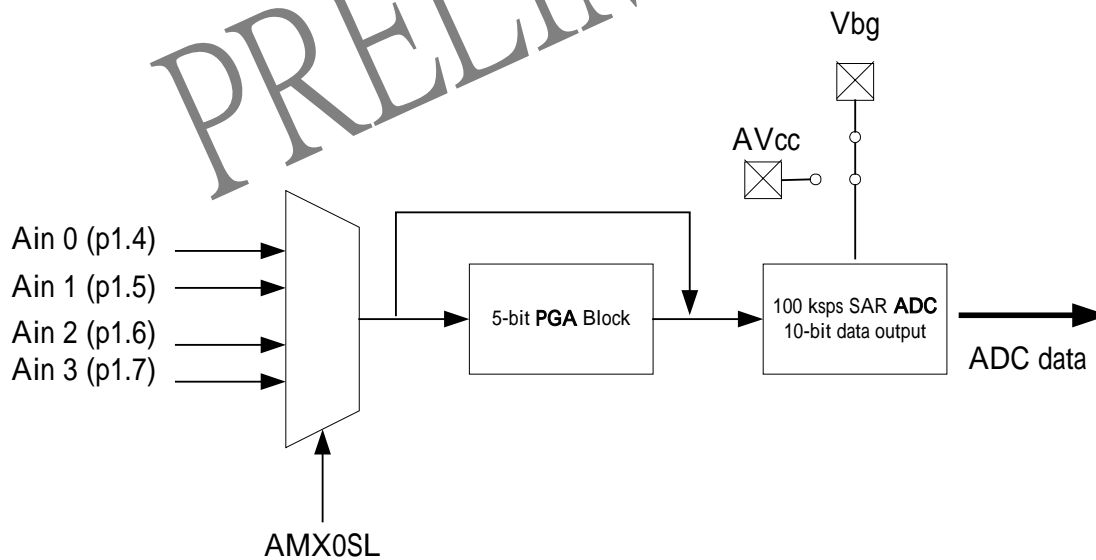


Figure8. ADC Diagram

**Figure 9. AMX0SL: AMUX Channel Select Register**

R	R	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	PINSL1	PINSL0	AIN3EN	AIN2EN	AIN1EN	AIN0EN	0000 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address AMX0SL: DBh

PINSL 1-0: Select one of 4 for analog input use.  
 00: P1.4 for analog input.  
 01: P1.5 for analog input.  
 10: P1.6 for analog input.  
 11: P1.7 for analog input.  
 AIN3EN: Set 0/1 to select P1.7 as digital/analog use.  
 AIN2EN: Set 0/1 to select P1.6 as digital/analog use.  
 AIN1EN: Set 0/1 to select P1.5 as digital/analog use.  
 AIN0EN: Set 0/1 to select P1.4 as digital/analog use.  
 For example: set "xx010010" to select P1.5 for analog input.  
 Bit 7-6 : Reserved for future use.

**Figure 10. ADC0PGA: ADC Programmable Amplify Register**

R	R	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	PGAEN	AMPGA4	AMPGA3	AMPGA2	AMPGA1	AMPGA0	0000 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address ADC0CF: DCh

PGAEN:  
 0: PGA block is disabled. AMUX output bypass the PGA Block and directly connects to SAR input.  
 1: PGA block is enabled. 10-bit SAR ADC input is from PGA output.  
 AMPGN 4-0: ADC Internal Amplifier Gain.  
 00000: Gain = 0.5  
 00001: Gain = 0.5  
 00010: Gain = 1.0  
 00011: Gain = 1.5  
 00100: Gain = 2.0  
 .  
 .  
 .  
 11111: Gain = 15.5  
 Bit 7-6 : Reserved for future use.



## ADC MODE OF OPERATION

The ADC has a maximum conversion speed of 100ksps. The ADC conversion clock is derived from the system clock.

Divide ratios are supported by setting the ADC0CLK register. This is useful to adjust conversion speed to accommodate different system clock speeds.

A conversion can be initiated in one of two ways, depending on the programmed states of the ADC track-and-hold mode bit “ADCTM”. In its default state, the ADC input is continuously tracked, except when a conversion is in progress. The continuously tracked rate is adjustable by setting the ADC0SR register. Setting “ADCTM” to logic 1, tracking begins with a write of logic 1 to the bit “ADCBUSY”. A completed conversion causes an interrupt through the ADC flag “ADCIF”, or a status bit “ADCBUSY” can be polled in software to determine the end of conversion. The resulting 10-bit data word is latched into SFR registers upon completion of a conversion.

**Figure 11. ADC0CN: ADC Control Register**

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	ADCPWD	ADCTYP	ADCTM	ADCBUSY	ADCIF	ADWIF	ADCRJST	0100 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address ADC0CN: DAH

ADCPWD: ADC Power Down Bit.  
 0: ADC is active and ready for data conversions.  
 1: ADC is in low power shutdown.(default)

ADCTYP: If set, ADC Voltage reference is from power AVCC. If cleared, ADC Voltage reference is from band-gap. (default)

ADCTM: ADC Track Mode Bit.  
 0: When the ADC is active, tracking is continuous unless a conversion is in process.  
 1: When the ADC is active, tracking starts with the write of 1 to ADBUSY.

ADCBUSY: ADC Busy Bit.  
 If ADCTM = 0, ADCBUSY is read only for indicator of ADC converting. If ADCTM = 1, ADCBUSY is R/W bit.  
 Read 0: ADC conversion complete or no valid data has been converted since a reset.  
 1: ADC busy converting data.(cleared by hardware) The falling edge of ADCBUSY generates an interrupt when enabled.  
 Write 0: No effect.  
 1: Starts ADC conversion if ADCTM=1.

ADCIF: ADC Conversion Complete Interrupt Flag. (Cleared by software)  
 0: ADC has not completed a data conversion since the last time this flag was cleared.  
 1: ADC has completed a data conversion.

ADWIF: ADC Window Compare Interrupt Flag. (Cleared by software)

ADCRJST: ADC Right Justify Data Bit.  
 0: Data in ADC0H: ADC0L registers are left justified. ADC0H[7:0]:ADC0L[7:6] for 10-bit ADC output.  
 1: Data in ADC0H: ADC0L registers are right justified. ADC0H[1:0]:ADC0L[7:0] for 10-bit ADC output.

Bit 7: Reserved for future use.

**Figure 12. ADC0CLK: ADC Conversion CLK Register**

R	R	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	ADCD5	ADCD4	ADCD3	ADCD2	ADCD1	ADCD0	0000 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address ADC0CLK: DDh

ADCD 5-0: ADC SAR Conversion Clock Period Bits.  
 $ADC\_Clock = SYS\_CLK / (ADCD[5:0] + 1)$   
 Bit 7-6 : Reserved for future use.

**Figure 13. ADC0SR: ADC Sample Rate Register**

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
ADSR7	ADSR6	ADSR5	ADSR4	ADSR3	ADSR2	ADSR1	ADSR0	0000 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address ADC0SR: DEh

ADC Sample Rate Register:  $Sample\ Rate = ADC\_Clock / (ADSR[7:0] + 1)$ , where  $sample\ rate \leq ADC\_CLK / 15$

**Figure 14. ADC0H,L: ADC Data Word Register**

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								0000 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address ADC0L: DFh

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								0000 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address ADC0H: E2h

[ADC0H:ADC0L]: ADC 10-bit Data Word Bits.  
 $ADC0H[7:0]:ADC0L[7:6]$  for 10-bit ADC output if  $ADCRJST = 0$ .  
 $ADC0H[1:0]:ADC0L[7:0]$  for 10-bit ADC output if  $ADCRJST = 1$ .

## ADC WINDOW DETECTOR

The ADC window detector is very useful in many applications. It continuously compares the ADC output to user-programmed limits and notifies the system when an out-of-band condition is detected. The window detector interrupt flag ("ADWINT") can also be used in polled mode. The high and low bytes of the reference words are loaded into the ADC Greater-Than and ADC Less-Than registers (ADC0GTh, ADC0GTL, ADC0LTH, and ADC0LTL). Notice that the window detector flag can be asserted when the measured data is inside or outside the user-programmed limits, depending on the programming of the ADC0GTH/L and ADC0LTH/L register pairs.

**Figure 15. ADC0GTH,L: ADC Greater-Than Data Word Register**

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								1111 1111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address
								ADC0GTL: E3h
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								1111 1111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address
								ADC0GTH: E4h

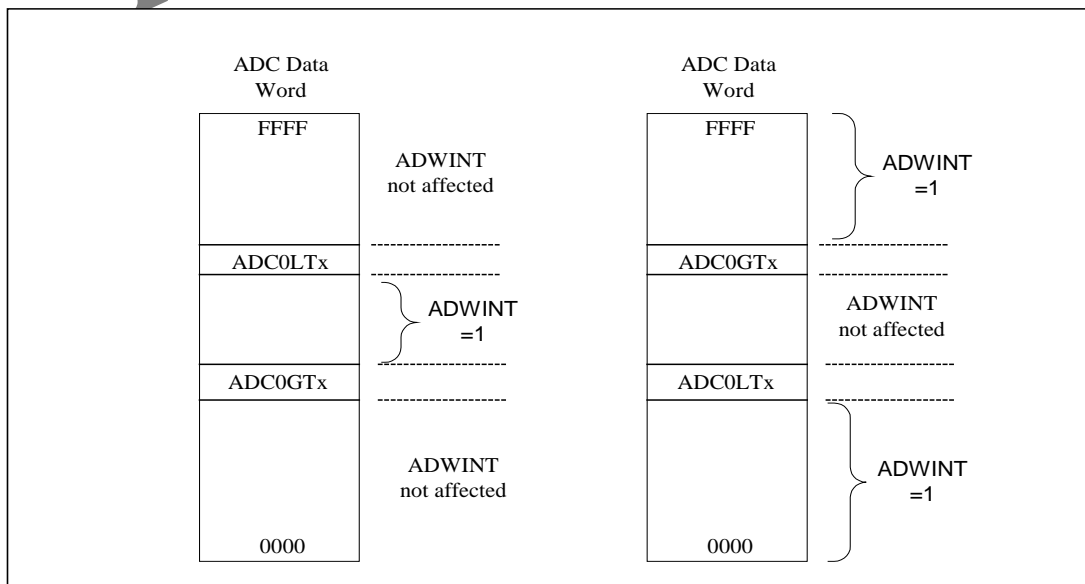
ADC Greater-Than Data Word = ADC0GTH: ADC0GTL  
 ADC0GTH[7:0]:ADC0GTL[7:6] for 10-bit ADC window comparer if ADCRJST = 0.  
 ADC0GTH[1:0]:ADC0GTL[7:0] for 10-bit ADC window comparer if ADCRJST = 1.

**Figure 16. ADC0LTH,L: ADC Less-Than Data Word Register**

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								0000 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address
								ADC0LTL: E5h
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								0000 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address
								ADC0LTH: E6h

ADC Less-Than Data word = ADC0LTH: ADC0LTL  
 ADC0LTH[7:0]:ADC0LTL[7:6] for 10-bit ADC window comparer if ADCRJST = 0.  
 ADC0LTH[1:0]:ADC0LTL[7:0] for 10-bit ADC window comparer if ADCRJST = 1.

**Figure 17. ADC Window Interrupt Examples**



## 10-BIT DAC

The AP180 incorporates two on-chip 10-bit, voltage output DACs. The DAC0 and DAC1 can be programmed independently by setting their own control bits. The DAC can be software-programmed for the conversion rate, that its maximum rate is 100ksp/s. The voltage reference can be the AVCC or Vbg depending on the bits “DACTYP”. The DAC is in low power shutdown when the bit “DACPWD” is set to logic 1.

To set the data output enable bits “DAC0/IOE” to logic 1, the DAC0/1 converts the digital value in DAC0/1 data word to voltage output in the pin P10/P11. An external audio amplifier and optional volume control must be used to driver a speaker.

**Figure 18. DACON: DAC Control Register**

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
DAC1PWD	DAC0PWD	DAC1OE	DAC0OE	DAC1TYP	DAC0TYP	DAC1RJST	DAC0RJST	1100 000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address
DACON: EAh								
<p>DAC1PWD: DAC1 Power Down Bit. Set it to 1, DAC1 is in low power shutdown.(default) Clear it to 0, DAC1 is active.</p> <p>DAC0PWD: DAC0 Power Down Bit. Set it to 1, DAC0 is in low power shutdown. (default) Clear it to 0, DAC0 is active.</p> <p>DAC1OE: DAC1 conversion trigger bit.</p> <p>If set, DAC1(DAC1H &amp; DAC1L) are shifted to DAC1 Buffer and begins to convert. When shift operation is complete, DAC1OE is cleared by hardware. (2 clks)</p> <p>DAC0OE: DAC0 conversion trigger bit.</p> <p>If set, DAC0(DAC0H &amp; DAC0L) are shifted to DAC0 Buffer and begins to convert. When shift operation is complete DAC0OE is cleared by hardware. (2 clks)</p> <p>DAC1TYP: If set, DAC1 Voltage reference is from power AVCC. If cleared, DAC1 Voltage reference is from band-gap.</p> <p>DAC0TYP: If set, DAC0 Voltage reference is from power AVCC. If cleared, DAC0 Voltage reference is from band-gap.</p> <p>DAC1RJST: DAC1 Right Justify Data Bit.</p> <p>0: Data in DAC1H:DAC1L registers are left justified. DAC1H[7:0]:DAC1L[7:6] for 10-bit DAC1 output.</p> <p>1: Data in DAC1H:DAC1L registers are right justified. DAC1H[1:0]:DAC1L[7:0] for 10-bit DAC1 output.</p> <p>DAC0RJST: DAC0 Right Justify Data Bit.</p> <p>0: Data in DAC0H:DAC0L registers are left justified. DAC0H[7:0]:DAC0L[7:6] for 10-bit DAC0 output.</p> <p>1: Data in DAC0H:DAC0L registers are right justified. DAC0H[1:0]:DAC0L[7:0] for 10-bit DAC0 output.</p>								

**Figure 19. DACxH,L: DAC0/DAC1 Data Word Register**

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								0000 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address
								DAC0L: EBh
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								0000 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address
								DAC0H: ECh
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								0000 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address
								DAC1L: EDh
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								0000 0000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address
								DAC1H: EEh

[DAC0H:DAC0L]: DAC0 10-bit Data Word Bits.  
 DAC0H[7:0]:DAC0L[7:6] for 10-bit DAC0 input if DAC0RJST = 0.  
 DAC0H[1:0]:DAC0L[7:0] for 10-bit DAC0 input if DAC0RJST = 1.

[DAC1H:DAC1L]: DAC1 10-bit Data Word Bits.  
 DAC1H[7:0]:DAC1L[7:6] for 10-bit DAC1 input if DAC1RJST = 0.  
 DAC1H[1:0]:DAC1L[7:0] for 10-bit DAC1 input if DAC1RJST = 1.

**Table8. ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VCC	-0.3	+3.6	V
Analog Supply Voltage	AVCC	-0.3	+3.6	V
Input Voltage	V <sub>IN</sub>	-0.5	VDD+0.5	V
Operating Temperature	T <sub>OPR</sub>	-25	+85	
Storage Temperature	T <sub>STG</sub>	-55	+125	

**Table9. DC ELECTRICAL CHARACTERISTICS**

(TA = -25°C to +85°C and VDD = 3.0V to 3.6V, unless otherwise specified)

Parameter	Symbol	Min.	Max.	Unit	Conditions
Input High Voltage (TTL input)	V <sub>IH</sub>	0.2VDD+0.9	VDD+0.2	V	
Input High Voltage (Schmitt input)	V <sub>IH1</sub>	0.7VDD	VDD+0.2	V	
Input Low Voltage	V <sub>IL</sub>	-0.5	0.2VDD-0.1	V	
Output Low Voltage; Port 1 and 3 (except P3.6 and P3.7)	V <sub>OL</sub>	-	0.4	V	I <sub>OL</sub> = 3.0mA; VDD = 3.0V
Output Low Voltage; Port 0 and 2, ALE, P3.6(WR), P3.7(RD)	V <sub>OL1</sub>	-	0.4	V	I <sub>OL1</sub> = 6.0mA; VDD = 3.0V
Output High Voltage Port 0, 1, 2, and 3, ALE	V <sub>OH</sub>	VDD-1.0	-	V	I <sub>OH</sub> = -20uA; VDD = 3.0V
Output High Voltage; Port 1 and 3 (except P3.6 and P3.7)	V <sub>OH1</sub> *1	VDD-0.5	-	V	I <sub>OH1</sub> = -3.0mA; VDD = 3.0V
Output High Voltage; Port 0 and 2, ALE, P3.6(WR), P3.7(RD)	V <sub>OH2</sub> *1	VDD-0.5	-	V	I <sub>OH1</sub> = -6.0mA; VDD = 3.0V
Internal Reset Pull-Down Resister	R <sub>RST</sub>	50	150	KΩ	
Input/Output Capacitance	C <sub>IO</sub>	-	10	pF	
Input Leakage Current	I <sub>LI</sub>	-	5	μA	V <sub>IN</sub> = 0.45V to VDD
Operating Current	I <sub>CC</sub>	-	30	mA	F <sub>sys</sub> = 16MHz, 3.6V
Supply Current, Idle Mode, Analog Function Disable	I <sub>ID</sub>	-	12	mA	F <sub>sys</sub> = 16MHz, 3.6V
Supply Current, Power down Analog Function Disable	I <sub>PD</sub>	-	5	μA	3.6V

**Note:**

\*1. When addressing external memory or during a 0-to-1 transition (A one-shot drives the ports hard for one clock cycles).

**Table10. A/D CONVERTER DC ELECTRICAL CHARACTERISTICS**  
(TA = -25°C to +85°C, VDD = 3.3V, AVDD = 3.3V)

Parameter	Symbol	Min.	Max.	Unit	Conditions
<b>Static Characteristics</b>					
Resolution	R	-	10	Bits	
<b>Dynamic Characteristics</b>					
SAR Clock Frequency	F <sub>ADC</sub>		F <sub>SYS</sub>	MHz	
Conversion Time in SAR Clocks	T <sub>SAR</sub>	15	-	Clocks	
Sample/Hold Acquisition Time	T <sub>SH</sub>	1	-	μs	
Throughput Rate	R <sub>ADC</sub>	-	100	ksps	
<b>Analog Input Characteristics</b>					
Analog Input Voltage	V <sub>INA</sub>	0	2.40/AVDD	V	
Analog Input Capacitance	C <sub>IA</sub>	-	15	pF	

**Table11. D/A CONVERTER DC ELECTRICAL CHARACTERISTICS**  
(TA = -25°C to +85°C, VDD = 3.3V, AVDD = 3.3V)

Parameter	Symbol	Min.	Max.	Unit	Conditions
<b>Static Characteristics</b>					
Resolution	R	-	10	Bits	
Maximum Conversion Rate	R <sub>dac</sub>	-	100	ksps	
<b>Analog Output Characteristics</b>					
Analog Output Voltage	V <sub>INA</sub>	0	2.40/AVDD-Voffset	V	
Analog Output Loading (SPO pin)	R <sub>dal</sub>	10	-	KΩ	

## Timing Waveforms [1]

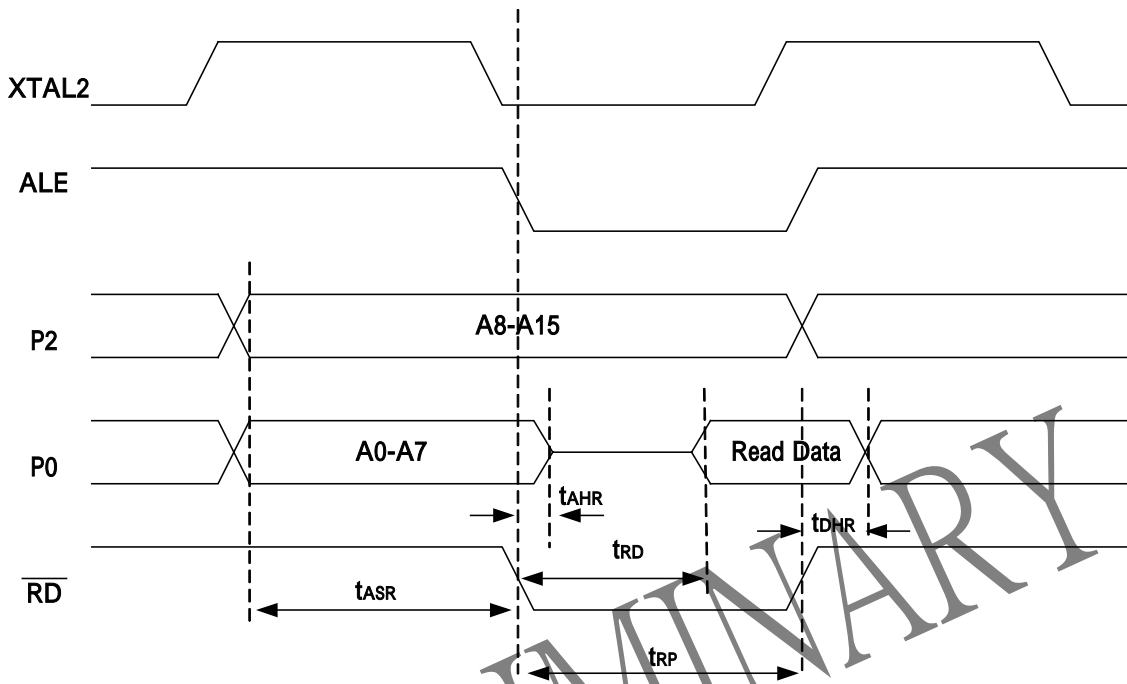


Figure 20. Data Memory Read Cycle

Table12-1. AC ELECTRICAL CHARACTERISTICS

(TA = -25°C to +85°C and VDD = 3.0V to 3.6V)

Parameter	Symbol	Min.	Max.	Unit
Address Setup to $\overline{RD}$ Low	tASR	TBD	TBD	ns
LSB Address Hold from $\overline{RD}$ Low	tAHR	TBD	TBD	ns
$\overline{RD}$ Pulse Width	tRP	TBD	--	ns
$\overline{RD}$ Low to Valid Data in	tRD	-	TBD	ns
Data Hold from $\overline{RD}$ High	tDHR	0	TBD	ns



## Timing Waveforms [2]

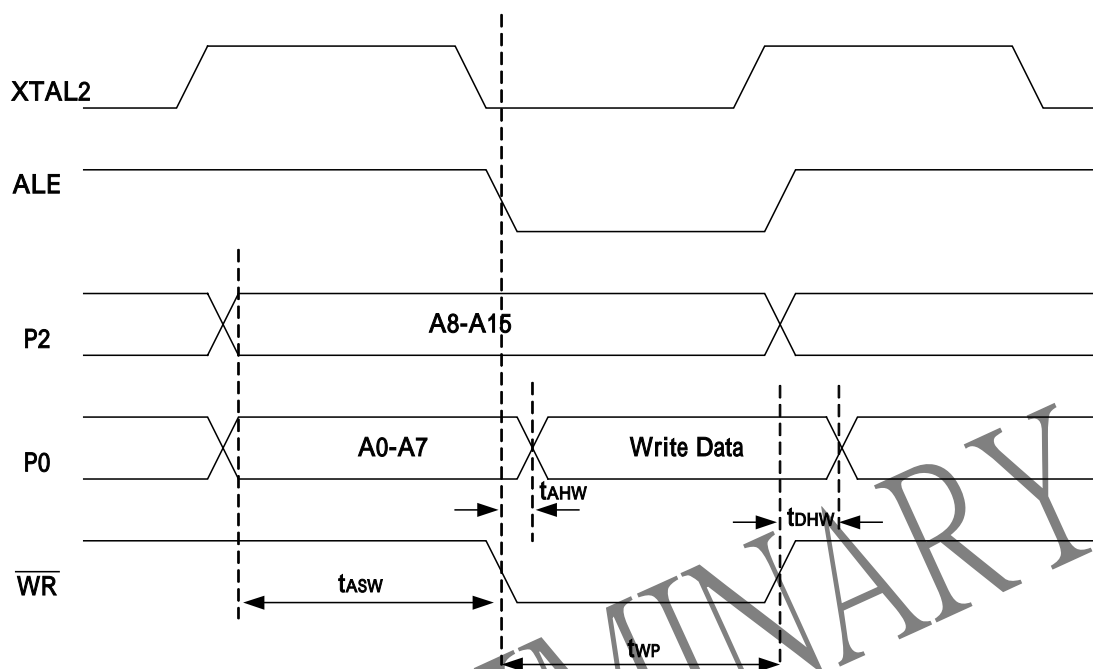


Figure21. Data Memory Write Cycle

## Table12-2. AC ELECTRICAL CHARACTERISTICS

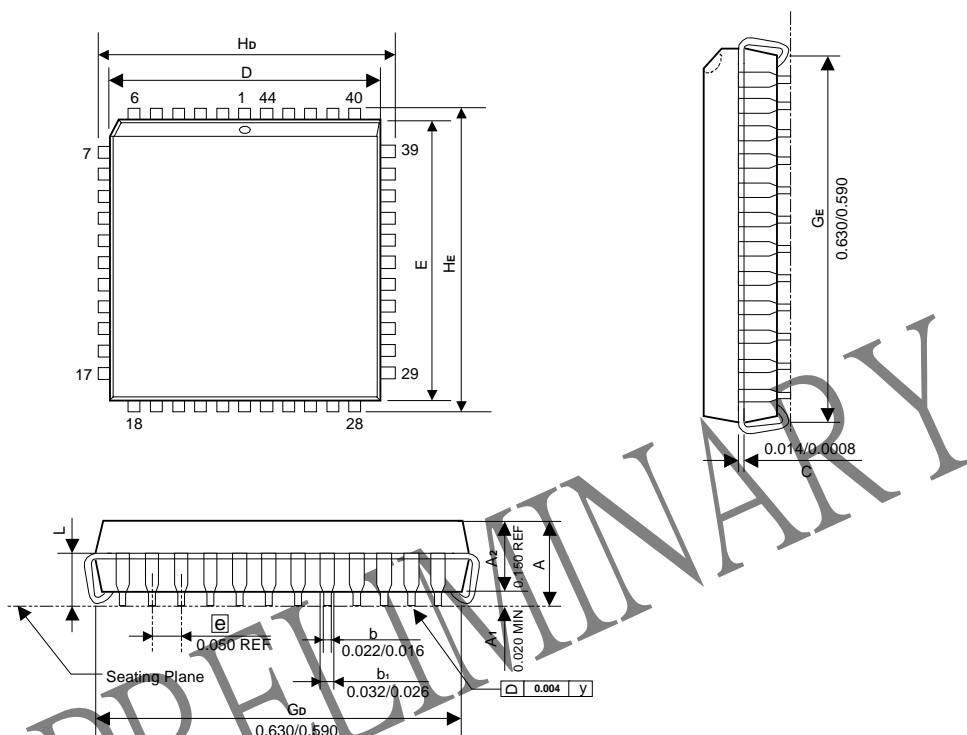
(TA = -25°C to +85°C and VDD = 3.0V to 3.6V)

Parameter	Symbol	Min.	Max.	Unit
Address Setup to $\overline{WR}$ Low	$t_{ASW}$	TBD	TBD	ns
LSB Address Hold from $\overline{WR}$ Low	$t_{AHW}$	TBD	TBD	ns
$\overline{WR}$ Pulse Width	$t_{WP}$	TBD	-	ns
Data Hold from $\overline{WR}$ High	$t_{DHW}$	0	TBD	ns

## PACKAGE INFORMATION

### PLCC 44L Outline Dimension

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.185	-	-	4.70
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
H <sub>D</sub>	0.680	0.690	0.700	17.27	17.53	17.78
H <sub>E</sub>	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.29	2.54	2.79
θ	0°	-	10°	0°	-	10°

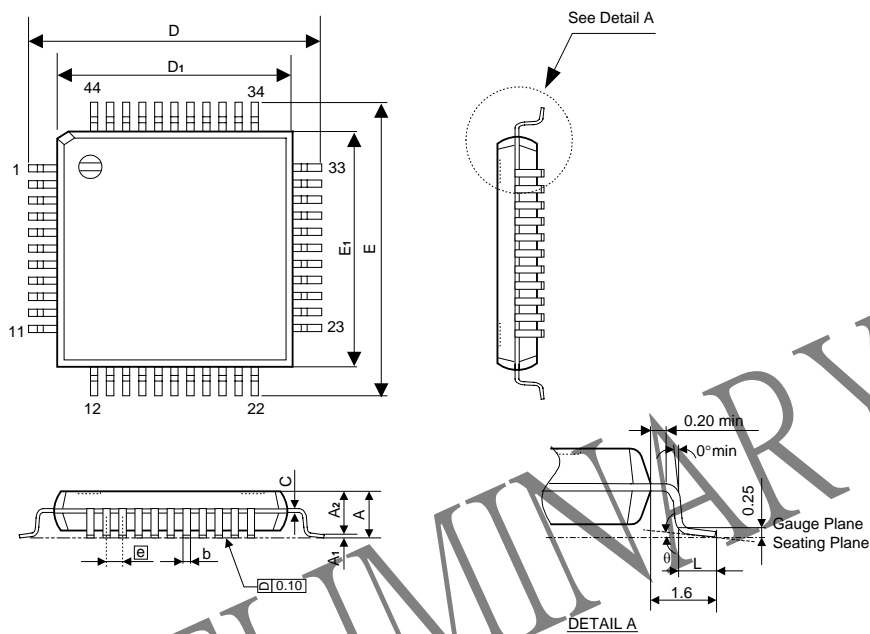
#### Notes:

1. Dimensions D and E do not include resin fins.
2. Dimensions G<sub>D</sub> & G<sub>E</sub> are for PC Board surface mount pad pitch design reference only.

## PACKAGE INFORMATION

### QFP 44L Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.106	-	-	2.7
A1	0.010	0.012	0.014	0.25	0.30	0.35
A2	0.0748	0.0787	0.0866	1.9	2.0	2.2
b	0.012 TYP			0.3 TYP		
D	0.5118	0.5196	0.5274	13.00	13.20	13.40
D1	0.3897	0.3937	0.3977	9.9	10.00	10.10
E	0.5118	0.5196	0.5275	13.00	13.20	13.40
E1	0.3897	0.3937	0.3977	9.9	10.00	10.10
L	0.0287	0.0346	0.0366	0.73	0.88	0.93
e	0.0315 TYP			0.80 TYP		
C	0.0021	0.0060	0.0099	0.1	0.15	0.2
θ	0°	-	7°	0°	-	7°

#### Notes:

1. Dimensions D1 and E1 do not include mold protrusion.
2. Dimension b does not include dambar protrusion.