



Application Notice Title

AP180 Parallel Programming Data

Revision History

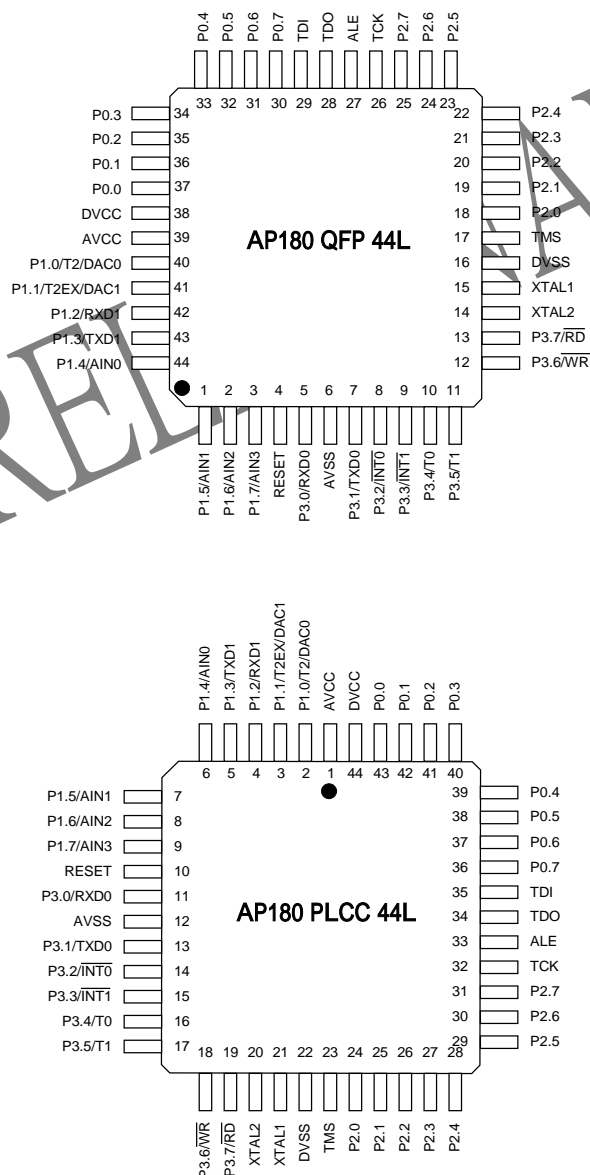
Rev.	History	Issue Date	Remark
1.0	Initial issue	April 27, 2004	Preliminary

PRELIMINARY

GENERAL DESCRIPTION

The AP180 offers the highest performance available in 8051-compatible microcontrollers. Its instructions are 100% binary compatible with the industry standard 8051. The same machine cycle takes 1 clock and it features a redesigned processor core that executes every 8051 instruction (depending on the instruction type) up to 12 times faster than the original for the same crystal speed.

Figure1. PIN CONFIGURATION



**AP180 ON-CHIP FLASH MEMORY**

There are two on-chip flash memory blocks for AP180. The full program memory size for main ROM code is 64KB which can be fetched by the processor automatically. There is also a separate 128 bytes flash memory for security use. Only 1 byte addressed 0000h is used to support a standard three-level lock options. The AP180 supports any of two programming methods as described in Table1. Serial programming is supported through the JTAG port. Parallel programming is provided with the programmer. This application note describes how to parallel programming the AP180 on-chip flash memory.

Table1. AP180 MODE SELECTION TABLE

External Pin Mode	Reset	ALE	P3.5	P3.0
Reset Mode	1	X	1	X
JTAG Mode (ICE & ISP)	0	X	X	X
Parallel Programming mode	1	0	0	1

Notes :

1. X=Either VIH or VIL..
2. “1” for logic high, and “0” for logic low.



SECURITY FEATURES

The AP180 supports three-level lock restricts viewing of the internal 64KB ROM code memory contents. By programming the two Lock-bit, the user can select a level of security as specified in Table2. But after AP180 device is powered-on, it is default restricted at level 3 and the user can not read or write 64KB memory through JTAG mode or on programmer. It needs read Lock-bit operation to reload the content of the Lock-bit. Only a mass erase can erase these bits to allow reprogramming the security level to a less restricted protection.

FLASH MEMORY LOCK-BIT

-	-	-	-	-	-	LB2	LB1	0000H
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Table2. LOCK BITS FEATURES

Level	LB2	LB1	Protection Type
1	U	U	No program lock feature enabled.
2	U	P	Data verification is disabled. (“Verify Signature Byte” and “Verify Lock Bits” are still enabled.)
3	P	P	Same as 2, also further written operation of the Flash is disabled.

Notes :

1. ‘U’= Non programmed or “1” level.
2. ‘P’= Programmed or “0” level

AP180 FLASH PARALLEL PROGRAMMING

The AP180 allows parallel programming of its internal flash memory on the programmers. In parallel programming mode, a mass-erase command with setting IFREN to logic high is used to erase both 64KB and the Lock-bit memory. If Lock-bit has not been programmed, the program code can be read back for verification. The state of the Lock-bit can also be verified directly in the parallel programming mode.

PARALLEL PROGRAMMING MODE SETTING

The interface for ROM flash is show in figure2. For Parallel Program Mode, “RESET” & “P3.0” pins keep at logic high, and “ALE” & “P3.5” pins keep at logic low. The pins TCK, TMS, TDI and TDO are not connected. To be programmed, the AP180 must be running with a 4MHz oscillator or greater.

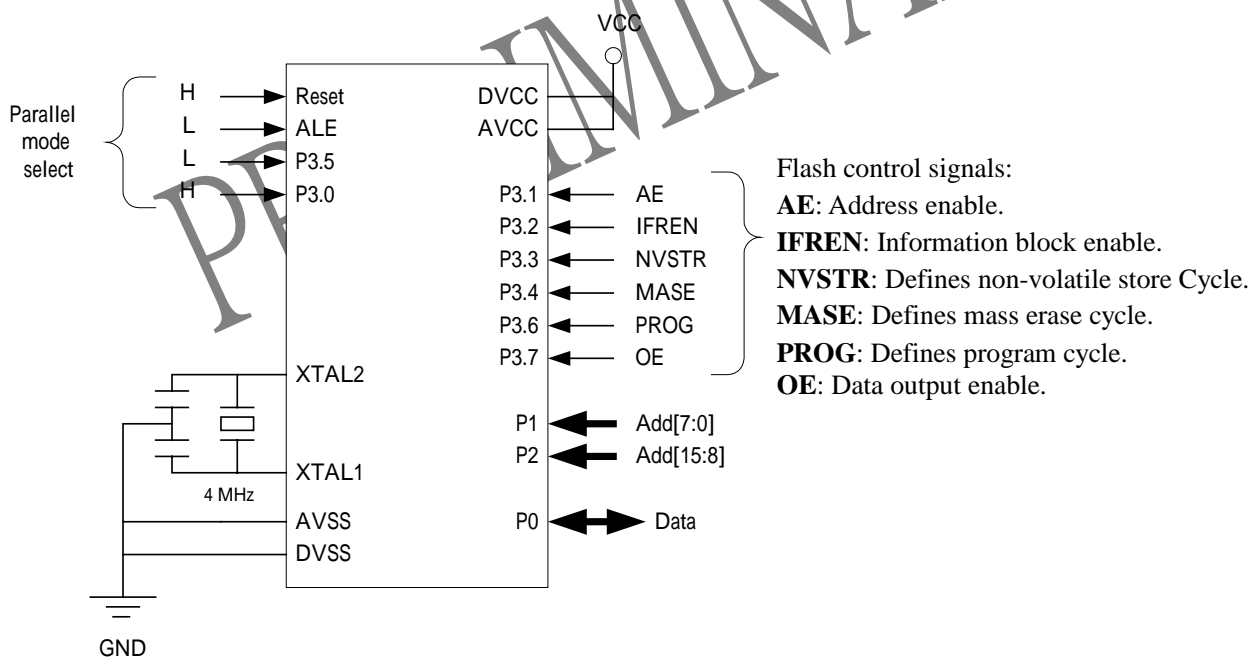


Figure2. AP180 Parallel Programming interface

**AP180 FLASH OPERATION****READ OPERATION**

To read data at the output, three control functions must be satisfied:

AE is the address enable and should pull high (VIH). Address will be valid after AE is high.

OE is the output enable and high active.

IFREN signal determines whether to read from 64KB main ROM memory or 128B memory.

BYTE PROGRAMMING OPERATION

The programming operation is a byte basis. **AE**, **PROG**, **NVSTR** and **IFREN** signals activate a program operation. The address and the data are latched on the rising edge of **PROG**. The internal programming voltages and timing is controlled by **NVSTR** signal.

A data "0" can not be programmed back to a "1". Only erase operation can convert "0"s to "1"s. A mass erase should be executed before the target array location being programmed.

MASE ERASE OPERATION

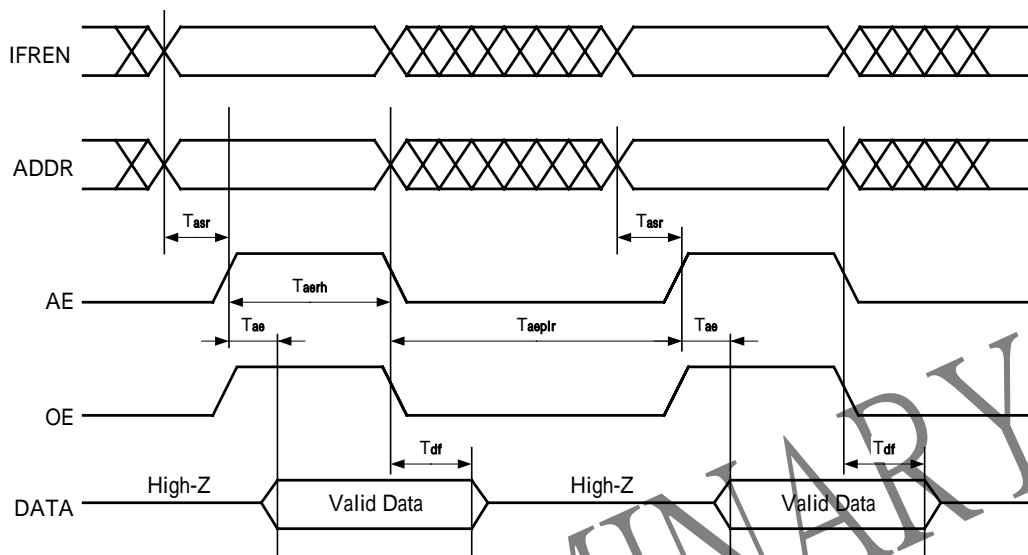
The entire memory array including both 64KB and 128B memory blocks can be erased through a mass erase operation. **AE**, **MASE**, **IFREN** and **NVSTR** signals active mass erase. The internal erasure voltage and timing is controlled by **NVSTR** signal.

Table4. USER MODE TRUTH TABLE FOR 64KB/128B FLASH MEMORY

Mode	AE	OE	PROG	MASE	NVSTR	IFREN	DATA	ADDRESS
Standby	L	X	X	X	X	X	Z	X
Read	H	H	L	L	L	active	Dout	active
Program	H	L	H	L	H	active	Din	active
Mase Erase	H	L	L	H	H	active	X	X

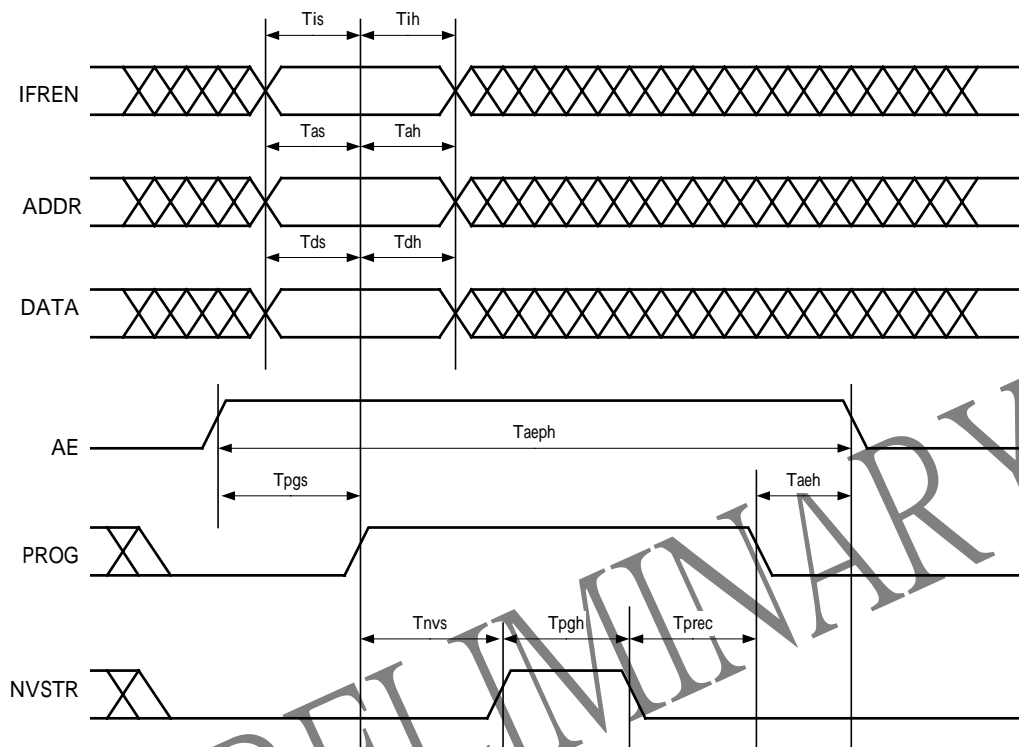
Table5. IFREN TRUTH TABLE

Mode	IFREN = 1	IFREN = 0
Read	Read 128B memory block	Read 64KB memory block
Program	Program 128B memory block	Program 64KB memory block
Mase Erase	Erase both blocks	Erase 64KB memory block

Timing Waveforms [1]

Figure 3. Read Operation Timings (AE Controlled)

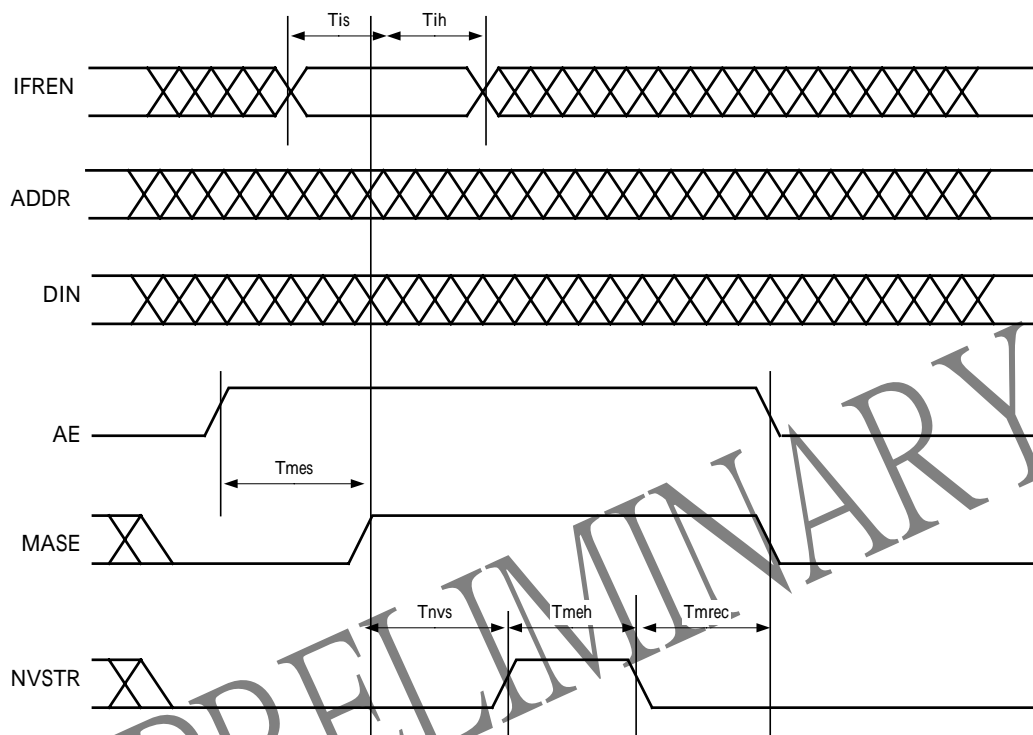
Parameter	Symbol	Min.	Max.	Unit
Address setup time at read	Tasr	0	-	ns
AE high and address hold time at read	Taerh	55	-	ns
AE access time at read	Tae	-	50	ns
AE pulse low hold time at read	Taeplr	10	-	ns
AE to output high Z	Tdf	-	10	ns

Note: During read operation, PROG, MASE and NVSTR are always logic L.

Timing Waveforms [2]

Figure 4. Program Operation Timings

Parameter	Symbol	Min.	Max.	Unit
Program setup time	T_{pgs}	20	-	ns
AE enable program hold time	T_{aeph}	20	-	us
NVSTR setup time	T_{nvs}	120	-	ns
Program hold time	T_{pgh}	20	40	us
Program recovery time	T_{prec}	3	-	us
AE hold time	T_{ah}	0	-	ns
IFREN setup time in program	T_{is}	0	-	ns
IFREN hold time in program	T_{ih}	20	-	ns
Address setup time	T_{as}	0	-	ns
Address hold time	T_{ah}	20	-	ns
Data setup time	T_{ds}	0	-	ns
Data hold time	T_{dh}	20	-	ns

Note: Program hold time can be 30 us for a typical value.

Timing Waveforms [3]

Figure 5. Mass Erase Operation Timings

Parameter	Symbol	Min.	Max.	Unit
Mase Erase setup time	Tmes	20	-	ns
NVSTR setup time	Tnvs	120	-	ns
Mase Erase hold time	Tmeh	40	80	ms
Mase Erase recovery time	Tmrec	100	-	us
IFREN setup time in Mase Erase	Tis	0	-	ns
IFREN hold time in Mase Erase	Tih	20	-	ns

Notes:

1. Mase Erase hold time can be 60 ms for a typical value.
2. Only support erase function for both memory blocks. (IFREN =1 when mase erase)



User interface for Programmer

For AP180 64KB memory block is used for ROM code, and 128B memory block is used for security bits. In fact security function is implemented by hardware lock bits. As IC Power ON, hardware lock bits default value are “00” for ROM code with Read and Write protection. It needs to read Lock-bit (in 128B memory block) to reload its value to hardware lock bits, so that power-on protection is released and user’s security set is active.

The functions for 64K bytes ROM memory block

1. Mase Erase: This operation erase both memory blocks. (IFREN =1 when mase erase) After this operation hardware lock bits are back to “11”.
2. Blank check: Check for both memory blocks.
3. Program: Byte programming following byte check. It needs once reading Lock-bit operation before program operation.
4. Verify: To verify 64K bytes with load file. It needs once reading Lock-bit operation before verification operation.
5. Read: To read 64K bytes to data buffer. It needs once reading Lock-bit operation before read operation.

The functions for 128 bytes information block (only 2 bits for security use)

There are three-level lock restricts for Flash ROM code by Programming lock bits:

1. Non programming LB1 and LB2 (LB2, LB1=11), 64K Flash ROM can be accessed for read and write operation.
2. To program LB1 (LB1=0), 64K Flash ROM is read protection and data output are all “FF”H.
2. To program both LB1 and LB2 (LB2, LB1=00), 64K Flash ROM is read and write protection. Only the mass erase operation can recover lock bits to allow reprogramming the security level to a less restricted protection.