Application Note AN_A8101_HW_01

General Information

Document Title

Application Note AN_A8101_HW_01

Revision History

Rev.	History	Issue Date	Remark
0.0	Initial issue	February, 2014	Preliminary
0.1	Modified pin configurations BP_BG to BG, VDD_H to REGI.	November, 2015	

Table of Contents

1. Crystal Selection Guide

To select an appropriate crystal for A8101 is important for good RF performance. If users are not familiar with how to choose the X'tal, we suggest them to use the one in BOM of MD8101-A05-12 module spec. The X'tal spec. shown in table 1 are some suitable examples. Users can also get more information in "*FQA_0001_Xtal Selection*". Users can adjust frequency by tuning the external capacitor at A8101 XI and XO pins or setting CSXTL in register [2A] DASP0. Please read A8101 datasheet or contact our FAE for detail.

Quartz Crystal Specification	**49S**
Center Frequency	16.384 MHz
Frequency tolerance at room temperature	±20 ppm
Frequency stability over operation temperature	±20 ppm
Load Capacitance	18 pF
Equivalent Series Resistor (ESR)	≦30Ω
Shunt Capacitance	5 pF
External Capacitor at A8101 XI pin	NC
External Capacitor at A8101 XO pin	NC
Crystal Setting Time(Typical)	0.6ms

Table 1 Quartz Crystal Specification

Annotation:

A8101 can works well with a X'tal with ESR < 80 Ω. However, the X'tal settling time will get longer with higher ESR. The X'tal shown in BOM of MD8101-A05-11 module spec. is fully tested. If users have problems with X'tal selection, please contact your X'tal supplier or Amiccom's FAE.

2. Application Circuit and Layout Guide

2.1 Application Circuit

MD8101-A05-12 is a reference design for wireless data transmission application (please see MD8101 module spec. for the newest update). The schematic is as Fig. 2.1a and main part of the layout is as Fig. 2.1b. This document mainly shows some key points which should be paid attention when doing layout.

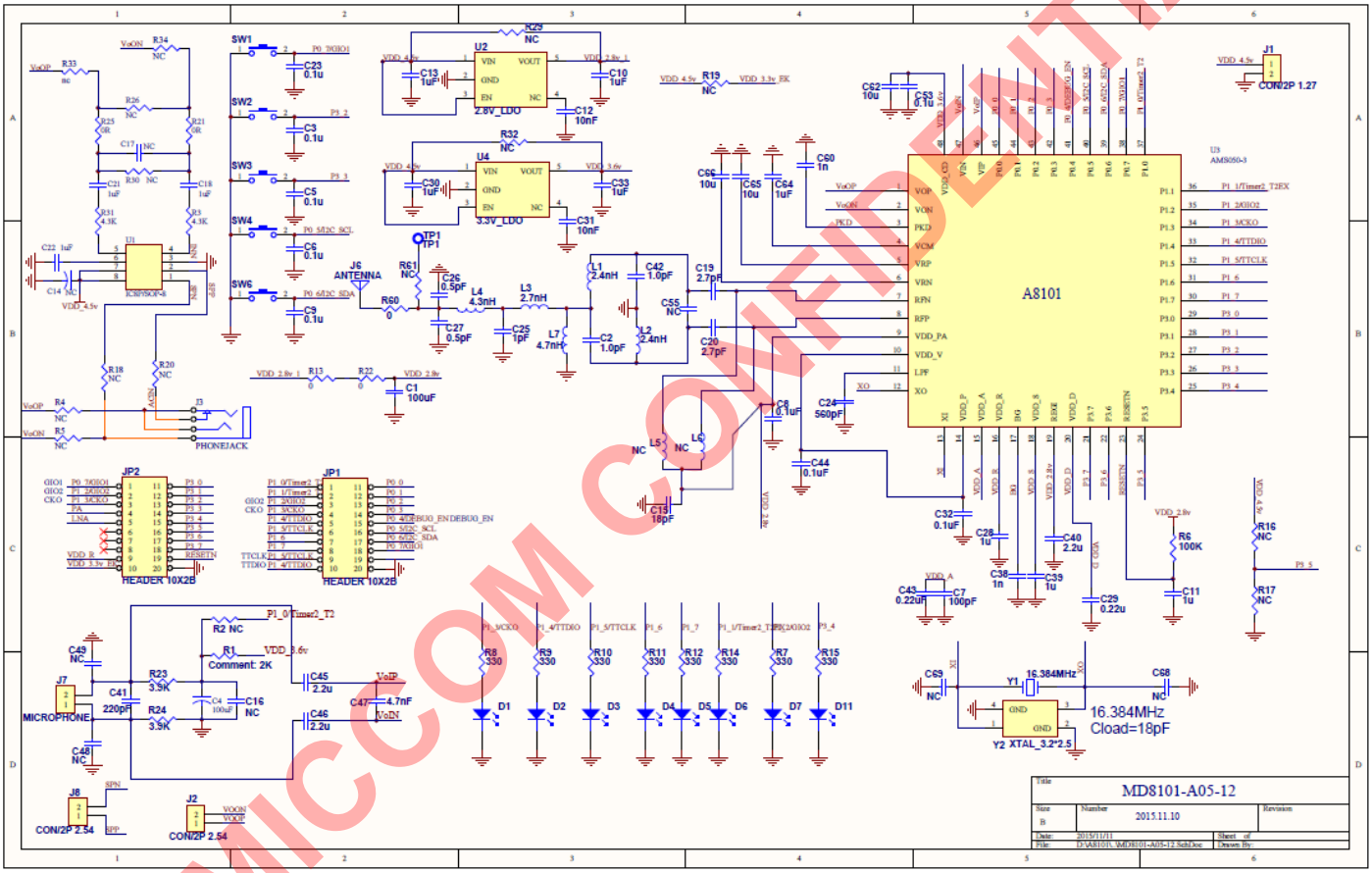

Fig. 2.1a Schematic of MD8101-A05-12

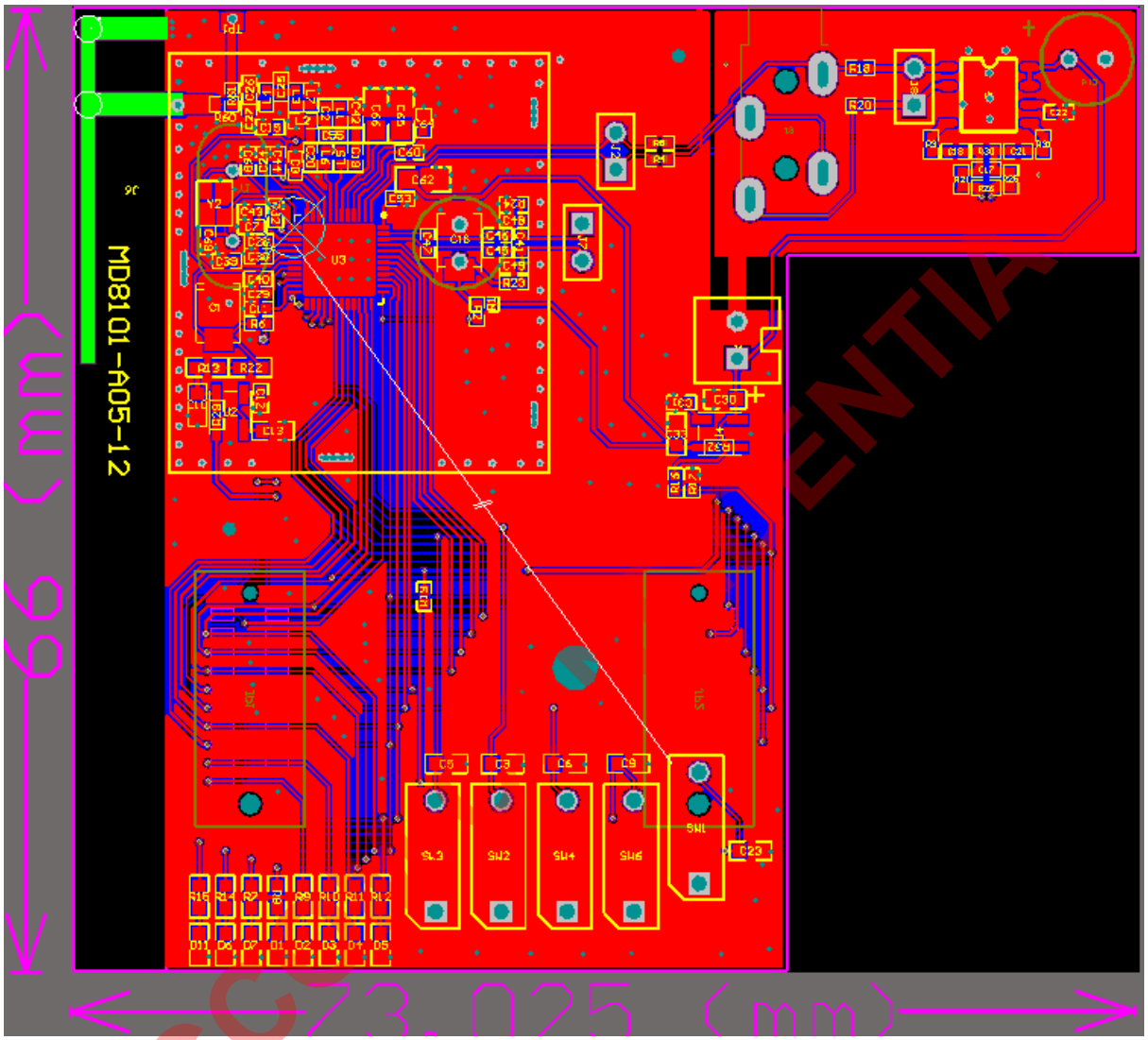

Fig. 2.1b Layout of MD8101-A05-12

2.2 Layout Guide

1. A8101 should have very solid ground. The ground plane should be intact, and not fragmentary. Please refer to Fig. 2.2a.

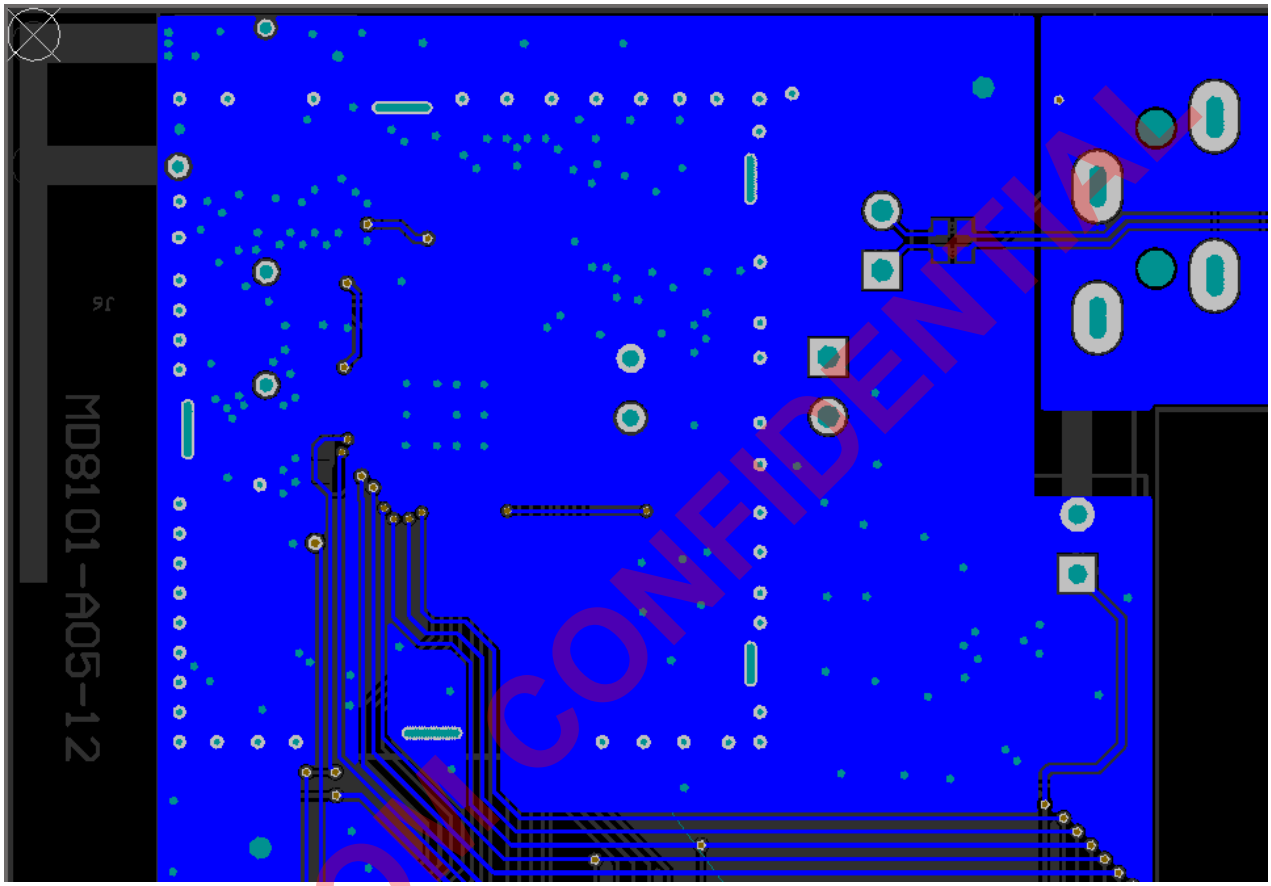

Fig. 2.2a Layout of MD8101-A05-12(Bottom view)

2. The impedance of RF path should as close to 50 ohm as possible, and the length also should be as short as possible. The ground plane below the RF traces should be intact and not fragmentary. The matching components (C19, C20, L1, L2, C2, C42) should be symmetric place and close to A8101 IC. Please refer to the green traces in Fig. 2.2b.

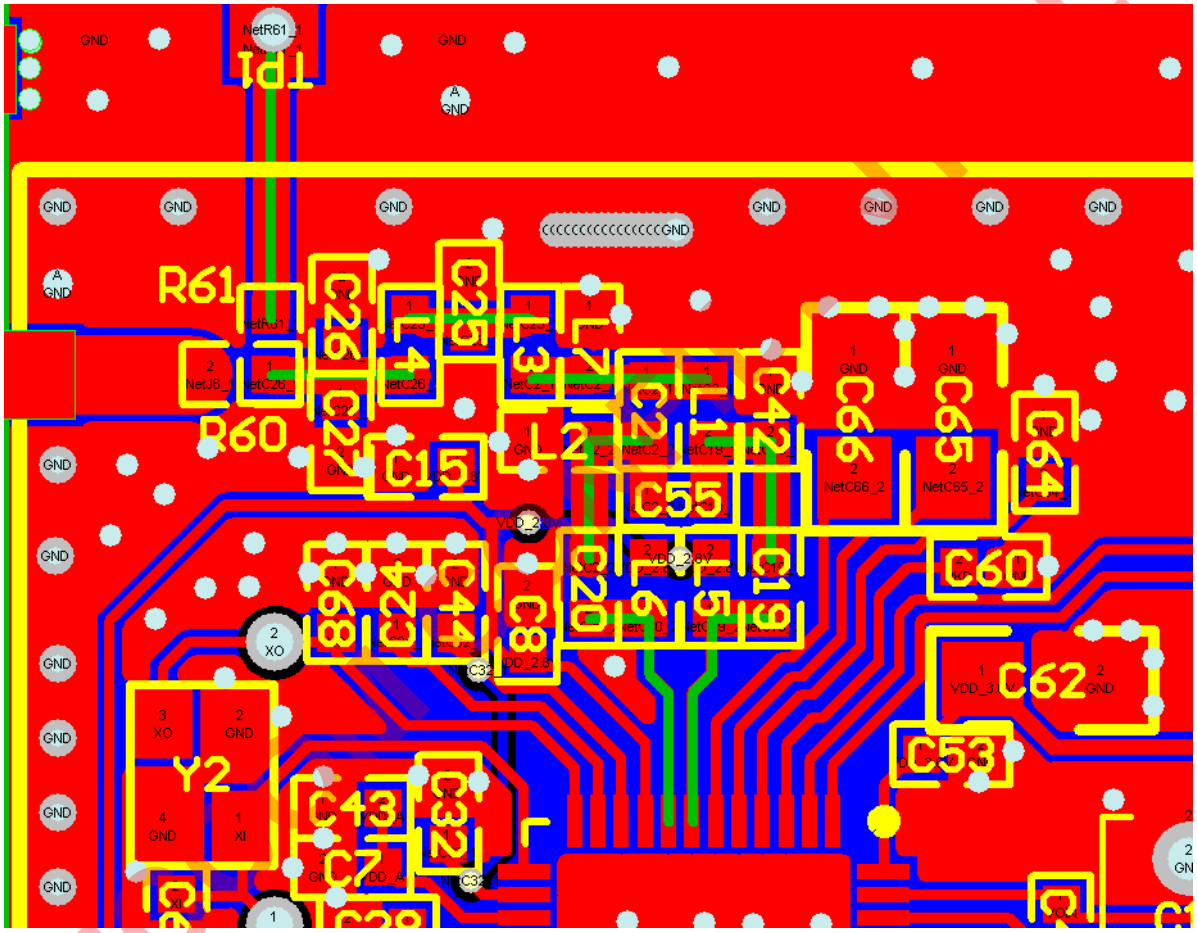

Fig. 2.2b 2.2b RF trace (green)

3. The bypass capacitors (C7, C8, C28, C29, C32, C38, C39, C40, C43, C44, C53, C60, C62, C64, C65, C66) should be very close the IC pins, and the ground via also should be very close the ground pad. Please refer to Fig. 2.2c.
4. The loop filter (C24) should be close to pin 11 of A8101 IC. Please refer to Fig. 2.2c.
5. The X'tal traces should be as short as possible and are better to be isolated by ground via. Please refer to the green traces in Fig. 2.2c.

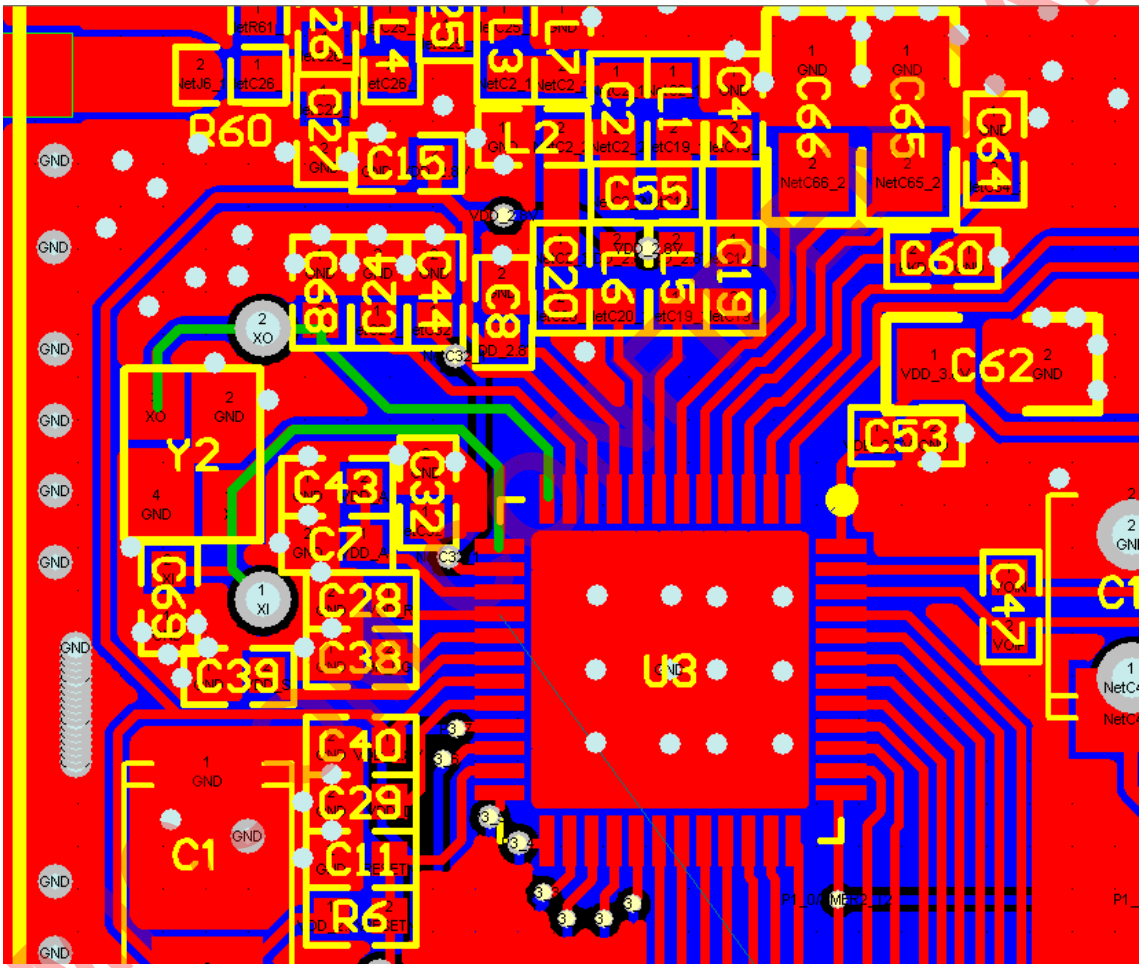

Fig. 2.2c X'tal trace (green)

6. The microphone input differential path (Pin 46: VIP and Pin 47: VIN) should be balanced and routed in parallel, as the same distance as possible from start to end. Please refer to the green traces in Fig. 2.2d.

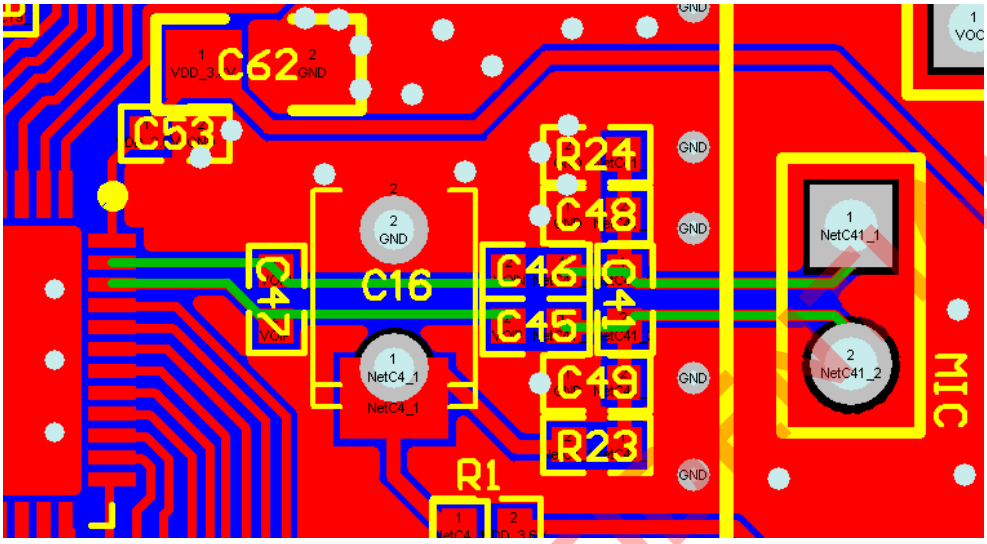

Fig 2.2d Microphone input trace(green)

7. The microphone should be far away from the PCB antenna to avoid the interference of high power RF signal. The microphone should be mount on PCB as close as possibly. Please refer to Fig. 2.2e.

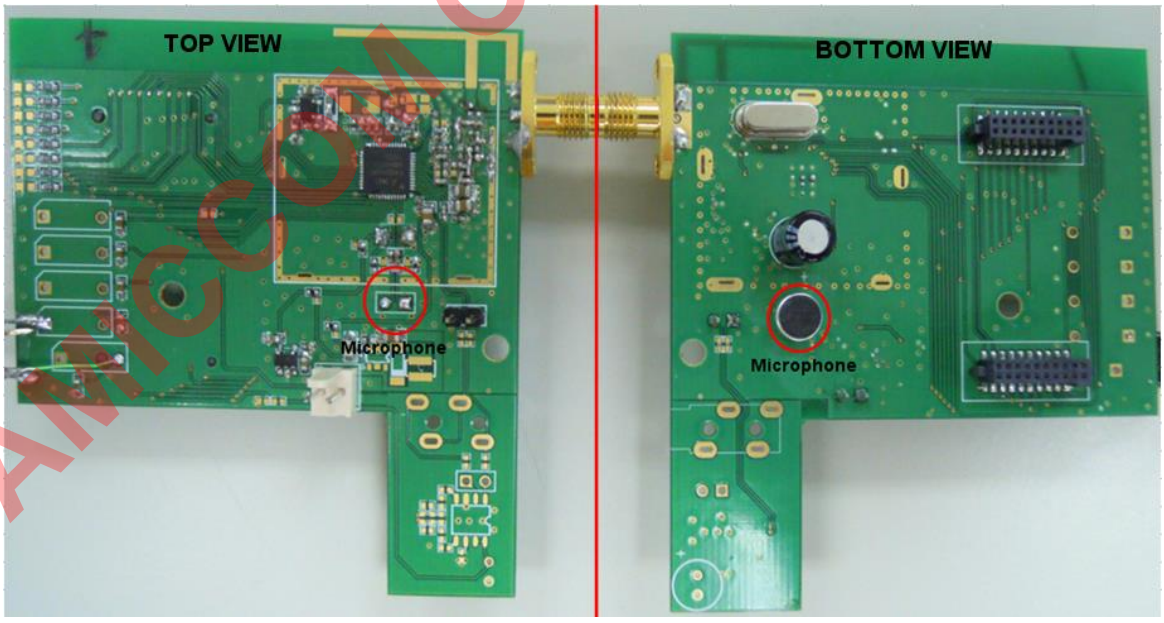

Fig 2.2e Microphone placement

8. The speaker output differential path (Pin 1: VOP and Pin 2: VON) should be balanced and routed in parallel, as the same distance as possible from start to end. Please refer to the green traces in Fig. 2.2f.

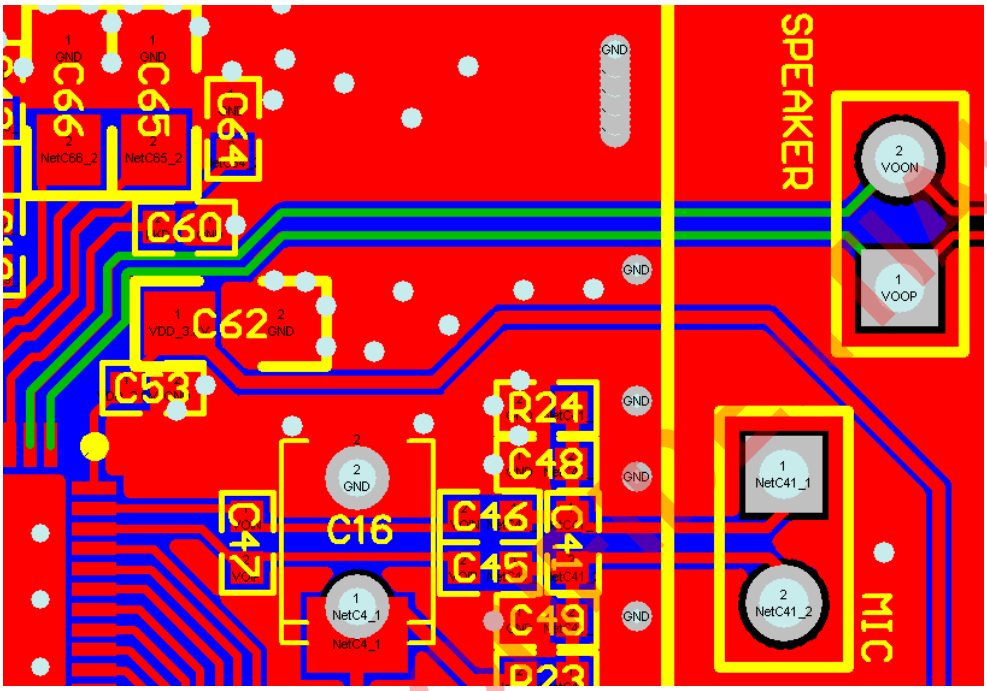

Fig 2.2f Speaker output trace(green)

9. The power lines supply of 2.8V LDO and 3.3V LDO, should be separated from the source power and routed independently. Please refer to the green traces in Fig. 2.2g

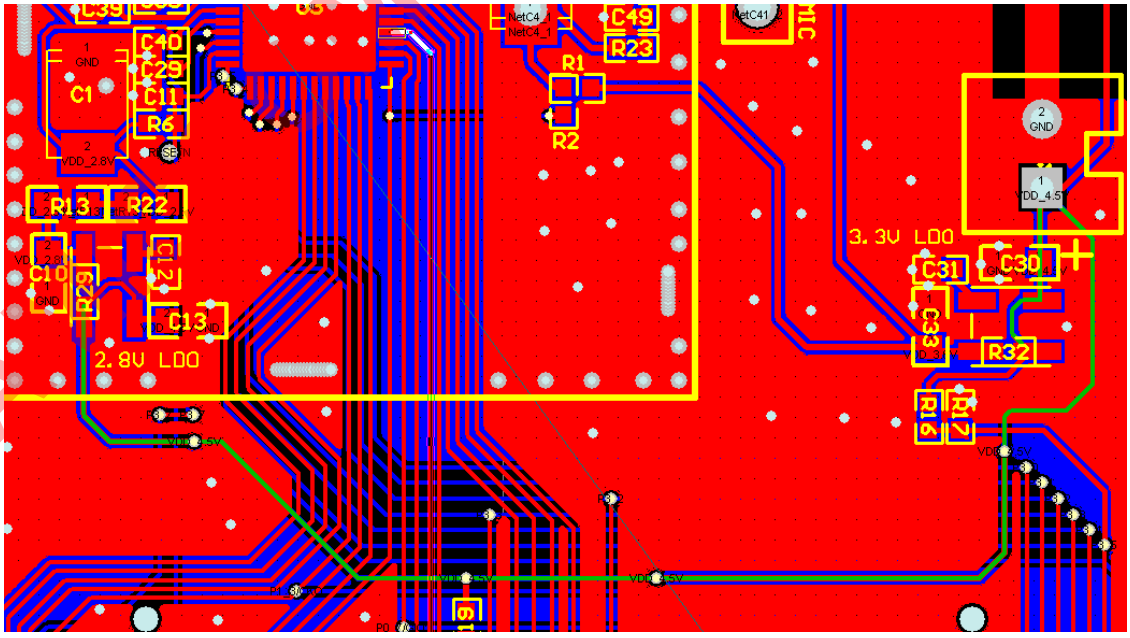

Fig 2.2g Power lines(green)

10. The 3.3V input power lines of microphone and pin 63(VDD_CD), should be separated from the 3.3V LDO output and routed independently. Please refer to the green traces in Fig. 2.2h

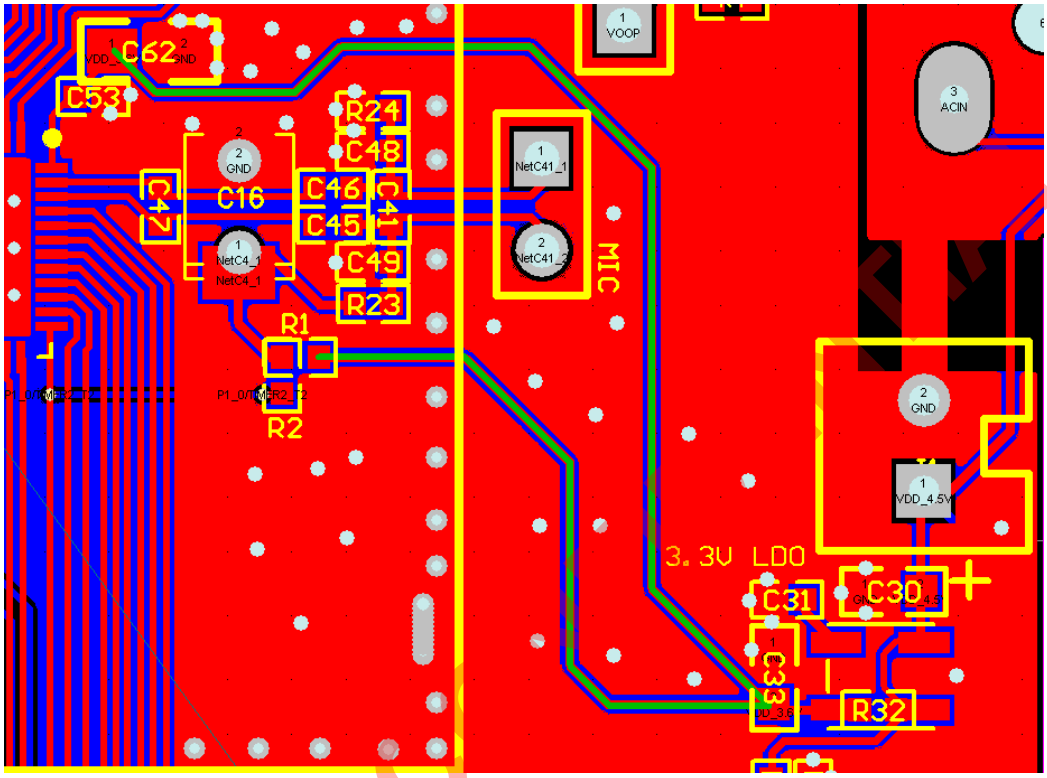

Fig 2.2h Power lines(green)

6.Tx Power Control Setting

Users can get different TX power by setting TBC (Tx Buffer current select), TDC (Tx driver current Select) and TPC (TX PA current Select) in register [0837] as the tables below. The default setting of register [0837] is 0x0D (TBC is set 0, TDC is set 0, TPC is set 1. The power maybe change between different modules because the variation of components.

3.1 Power control setting

TPC	TDC	TBC	Power(dBm)	Current(mA)	TPC	TDC	TBC	Power(dBm)	Current(mA)
3	3	3	20.11	160.33	2	3	3	19.87	154.67
3	3	2	19.9	156.33	2	3	2	19.64	150
3	3	1	19.51	150.33	2	3	1	19.23	143.67
3	3	0	18.66	142	2	3	0	18.37	133
3	2	3	19.8	154.33	2	2	3	19.55	148
3	2	2	19.54	149.67	2	2	2	19.26	142.67
3	2	1	19.04	143	2	2	1	18.74	135.33
3	2	0	17.99	134.33	2	2	0	17.71	124.33
3	1	3	19.82	146	2	1	3	18.99	138.33
3	1	2	18.89	140.67	2	1	2	18.59	132.67
3	1	1	18.19	134.33	2	1	1	17.88	124
3	1	0	16.82	125.67	2	1	0	16.58	113
3	0	3	18.18	135	2	0	3	17.89	124.67
3	0	2	17.56	130	2	0	2	17.28	118.33
3	0	1	16.47	123.33	2	0	1	16.26	110
3	0	0	14.61	116	2	0	0	14.49	101

TPC	TDC	TBC	Power(dBm)	Current(mA)	TPC	TDC	TBC	Power(dBm)	Current(mA)
1	3	3	19.55	148.67	0	3	3	19.07	141
1	3	2	19.29	143.33	0	3	2	18.74	135.33
1	3	1	18.82	136	0	3	1	18.15	127.33
1	3	0	17.87	124.67	0	3	0	16.96	113.67
1	2	3	19.16	141	0	2	3	18.57	132.33
1	2	2	18.83	135.33	0	2	2	18.16	126
1	2	1	18.25	127	0	2	1	17.4	116.67
1	2	0	17.11	114.33	0	2	0	16.04	103
1	1	3	18.52	130.67	0	1	3	17.73	120.33
1	1	2	18.06	124	0	1	2	17.16	113.33
1	1	1	17.27	114.67	0	1	1	16.19	103.33
1	1	0	15.91	102	0	1	0	14.62	89.67
1	0	3	17.28	115.33	0	0	3	16.21	104
1	0	2	16.62	108.33	0	0	2	15.43	96.67
1	0	1	15.57	98.67	0	0	1	14.23	86.33
1	0	0	13.86	87.33	0	0	0	12.37	74.33

Annotation:

The input voltage and P.A. voltage are 2.8V (REGI).

User can get more information from our FAE.

6. Sensitivity Flatness

Users can set different channel by setting CHN (channel number) in register [0811]. The default setting of register [0811] is 0x51 by 4M bps data rate. When Tx frequency is in the N*16MHz (X'tal frequcncy) ± 2MHz, the sensitivity will degrade a little because of the interference from the X'tal. We suggest customers avoid using these channels. Typical sensitivity flatness is shown in fig. 4.1.

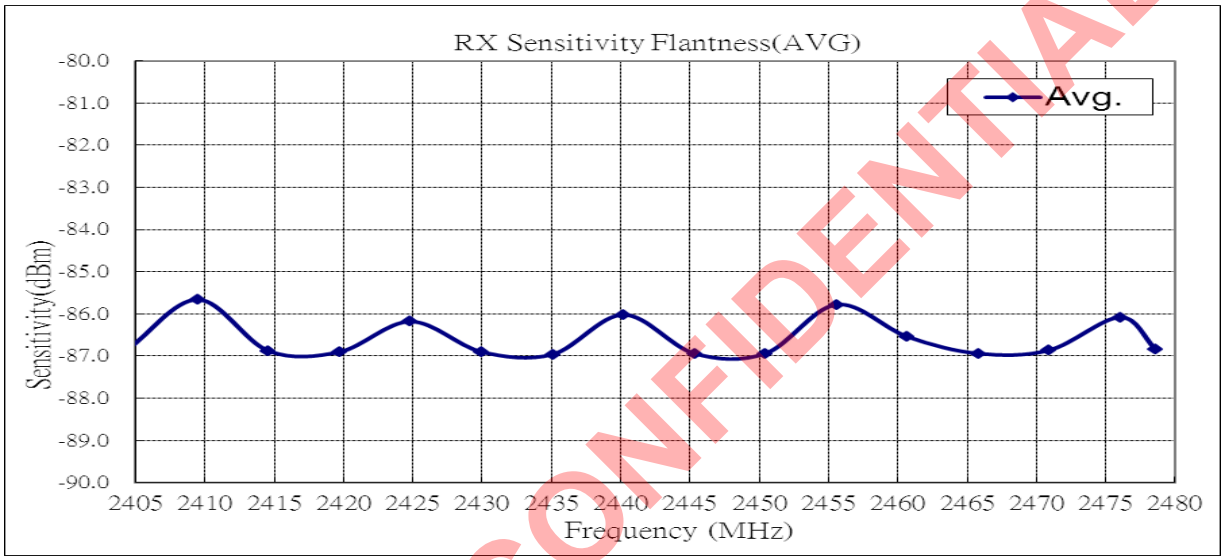

Fig. 4.1 Sensitivity flatness

7. RSSI

A8101has built-in digital RSSI (Received Signal Strength Indicator) which measure the strength of the incoming RF signal. The digital RSSI can be read form ED value and its range is form 0 to 255 (8bits). In the linear range, users can use the formula below to get the rough input power of the module.

Pin (dBm) = 12 * [(ED-RL) / (RH-RL)] – 80

ED, RL and RH value can be read from the registers.

The ADC values of each IC may have slight difference. If customers want to get more accurate RSSI value, they should use the ICs with RSSI tuning. Please contact Amiccom's FAE for detail about the RSSI tuning.

Typical RSSI characteristic is shown in fig. 5.1.

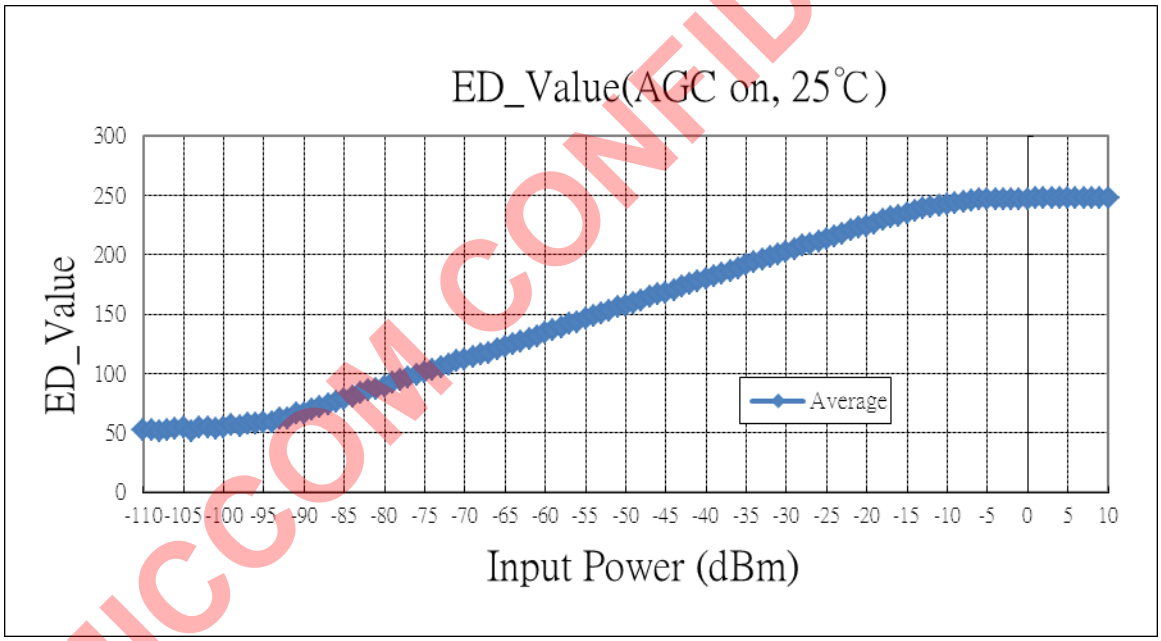

Fig. 5.1 RSSI curve

6. Temperature Curve

A7190 has a thermal sensor inside and users can know the rough temperature of the IC form reading the value of ADC.

If the ADC value at 25°C is X, and the ADC value we get is Y at certain temperature T, we can calculate T from the formula below roughly.

$$T\ (^{o}C) = 1.98\ (Y - X) + 25$$

The ADC values of each IC may have slight difference. If customers want to get more accurate Temp ADC value, they should use the ICs with Temp tuning. Please contact Amiccom's FAE for detail about the Temp tuning

Some measurement data is as Fig. 6.1 below.

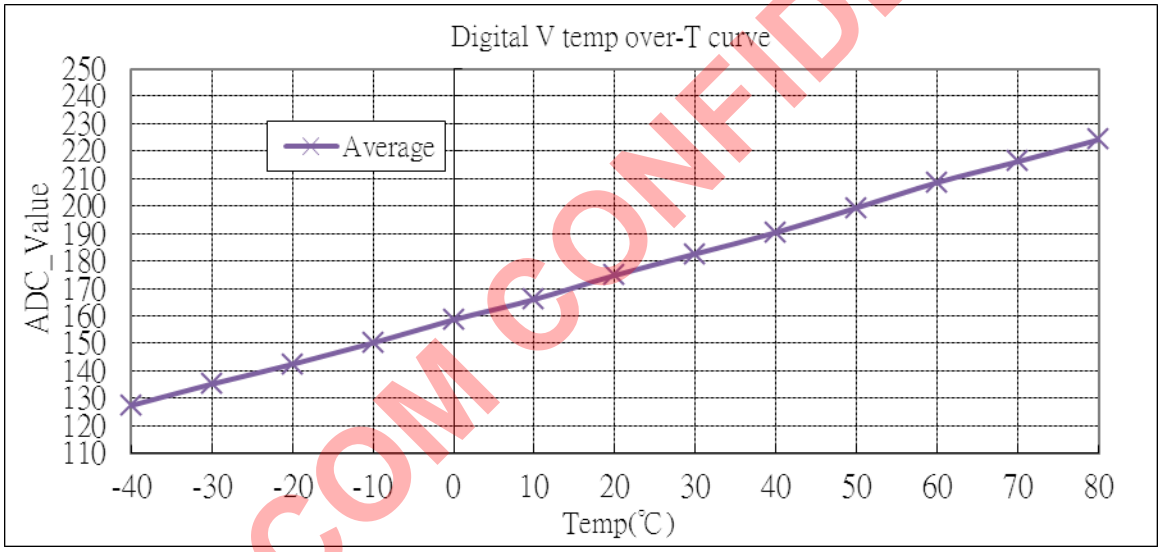

Fig. 6.1 Temperature curve