Document Title

A5133 Data Sheet, 5.8GHz 15dBm FSK Transceiver.

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue.	Jan., 2019	Objective
0.1	Change TX maximum output power. Delete deep sleep mode. Delete QFN5x5 package.	Apr., 2019	Preliminary
0.2	Update application circuit. Simplify chapter 14 LO frequency setting. Update current consumption and RX sensitivity specification. Update chapter 9 register. Update top marking information.	Sep., 2019	Preliminary
0.3	Modify TDL formula. Update application circuit.	Oct., 2019	Preliminary
0.4	Correct FEP bit number.	Nov., 2019	Preliminary
0.5	Update RH, RL, GIO1, GIO2 register.	Jun., 2020	Preliminary
0.6	Update chapter 7 input RF level.	Sep., 2021	Preliminary
0.7	Update RFP, RFN pin description.	Nov., 2021	Preliminary
0.8	Modify chapter 12 external clock description.	Jul., 2022	Preliminary
1.0	Full Production	Jan., 2023	
1.1	Modify Figure 19.3 WTR Behavior timing of Sender site.	Aug., 2023	

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1. General Description

A5133 is a low cost 5.8GHz band FSK transceiver. It supports data rate up to 4Mbps (FSK mode).

For packet handling, A5133 has built-in separated (64 bytes) TX/RX FIFO for data buffering and burst transmission, auto-ack and auto-resend, CRC for error packet filtering, FEC (7,4 hamming code) for 1-bit data correction per code word, RSSI for clear channel assessment, thermal sensor to monitor relative temperature, data whitening for data encryption / decryption. In addition, A5133 has built-in AES128 co-processor (Advanced Encryption Standard) for advanced data encryption or decryption which consists of the transformation of a 128-bit block into an encrypted 128-bit block. Those functions are very easy to use while developing a wireless system.

A5133's **control registers** are accessed via 3-wire or 4-wire SPI interface such as TX/RF FIFO, ID register, RSSI value, frequency hopping and calibration procedures. Another one is the unique **Strobe command** via SPI to control power saving mode (sleep, idle, standby), TX mode and RX mode. The other connections between A5133 and MCU are GIO1 and GIO2 (multi-function GPIO) to output A5133's status so that MCU could use either polling or interrupt scheme for radio control. Overall, it is very easy to develop a wireless application by a MCU and A5133 because of its rich and easy-to-use features.

2. Typical Applications

- HiFi quality wireless audio streaming
- Video streaming
- 5.8GHz band system
- Wireless toys and game controllers

3. Features

- Package size: QFN4x4 24 pins.
- FSK modulation.
- Sleep current (4uA).
- RX current consumption: 33 mA (AGC on).
- TX current consumption: 88 mA (15 dBm)
- On chip regulator, support input voltage 2 ~ 3.6V.
- Programmable data rate: Up to 4Mbps (FSK mode).
- Maximum TX output power: Up to 15 dBm.
- RX sensitivity: -91 dBm (FSK 4Mbps).
- Built-in AES128 co-processor.
- Easy to use.
  - Support 3-wire or 4-wire SPI.
  - Unique Strobe command via SPI.
  - ONE register setting for new channel frequency.
  - CRC Error Packet Filtering.
  - Auto-acknowledgement and auto-resend.
  - Separated 64Byte TX/RX FIFO.
  - 8-bits RSSI measurement for clear channel indication.
  - Auto Calibrations.
  - Auto IF function.
  - FEC by (7, 4) Hamming code (1 bit error correction / code word).
- Easy FIFO / Segment FIFO / FIFO Extension (up to 4K bytes).
  - Support FIFO mode frame sync to MCU.
  - Support direct mode with recovery clock output to MCU.

4. Pin Configurations

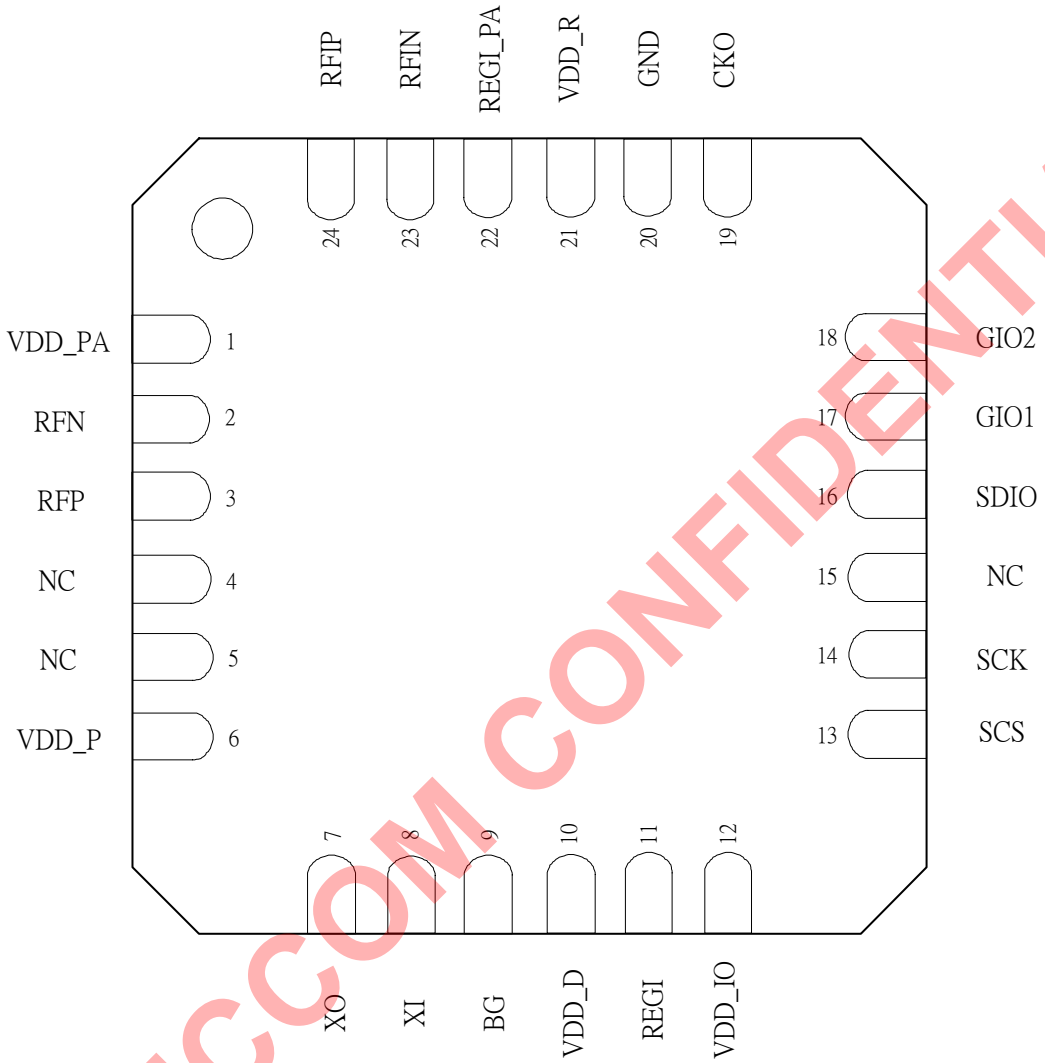


Figure 4.1 A5133 QFN4x4 24L Package Top View

5. Pin Descriptions (I: input; O: output, I/O: input or output)

Pin No.	Pin Name	I/O	Function Description
1	VDD_PA	AO	VDD_PA supply voltage output
2	RFN	AO	Negative RF output.
3	RFP	AO	Positive RF output.
4	NC		
5	NC		
6	VDD_P	AO	PLL supply voltage output.
7	XO	AO	Crystal oscillator output.
8	XI	AIO	Crystal oscillator input.
9	BG	AO	Band-gap output.
10	VDD_D	AO	VDD_D supply voltage output.
11	REGI	AI	Regulator input
12	VDD_IO	AI	VDD_IO supply voltage input
13	SCS	DI	SPI chip select input.
14	SCK	DI	SPI clock input.
15	NC		
16	SDIO	DIO	SPI data IO.
17	GIO1	DIO	Multi-function IO 1.
18	GIO2	DIO	Multi-function IO 2.
19	CKO	DO	Multi-function clock output.
20	GND	G	Ground.
21	VDD_R	AIO	Auxiliary supply for 8 bit ADC input circuit.
22	REGI_PA	AI	PA regulator input.
23	RFIN	AI	Negative RF input.
24	RFIP	AI	Positive RF input.
	Back side plate	G	Ground. Back side plate shall be well-solder to ground; otherwise, it will impact RF performance.

Table 5.1 QFN4x4 24 pins

6. Chip Block Diagram

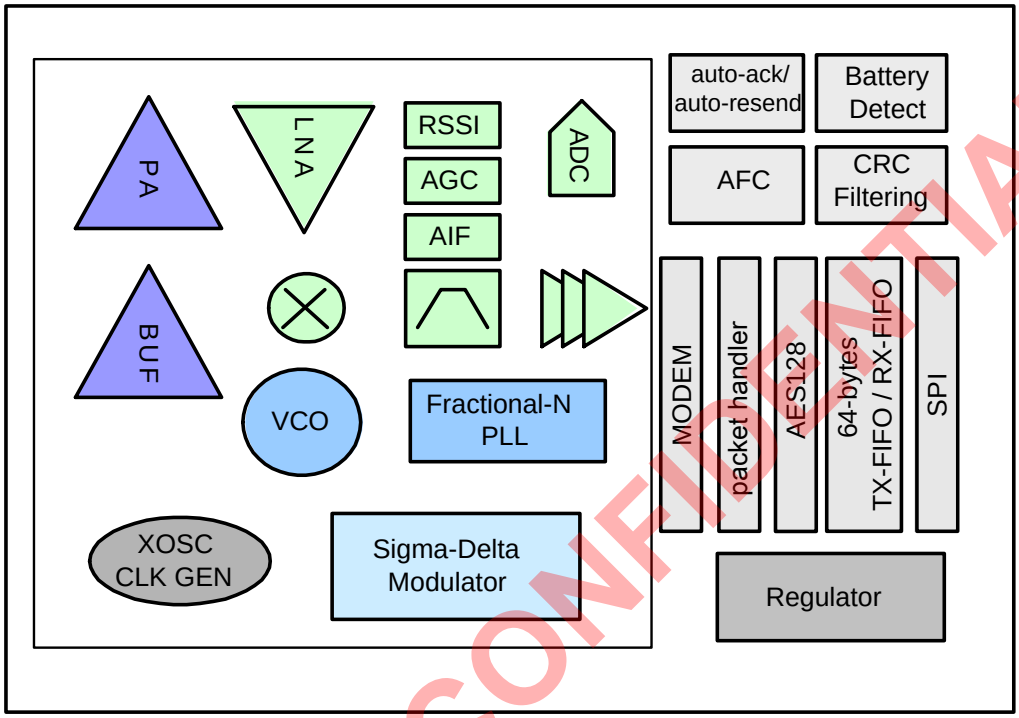


Figure 6.1 A5133 Block Diagram

7. Absolute Maximum Ratings

Parameter	With respect to	Rating	Unit
Supply Voltage range (VDD)	GND	-0.3 ~ 3.6	V
Digital IO pins range	GND	-0.3 ~ VDD+0.3	V
Input RF level		10	dBm
Storage Temperature range		-55 ~ 125	℃
ESD Rating	HBM	± 2K*	V
	MM	± 100*	V

*Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*Device is ESD sensitive. Use appropriate ESD precautions. HBM (Human Body Mode) is tested under MIL-STD-883F Method 3015.7. MM (Machine Mode) is tested under JEDEC EIA/JESD22-A115-A.
*Device is Moisture Sensitivity Level III (MSL 3).
*VDD_PA, RFN, RFP pin HBM is ± 1KV and MM is ± 50V.

8. Electrical Specification

(Ta=25℃, **VDD=3.3V**, F_{XTAL} =16MHz, with Matching and low pass filter, On Chip Regulator = **1.2V**, unless otherwise noted.)

Parameter	Description	Min.	Typ.	Max.	Unit
General					
Operating Temperature		-40		85	℃
Supply Voltage (VDD)		2	3.3	3.6	V
Current Consumption	Sleep mode (IRC on)*[1]		4		uA
	Idle Mode (Regulator on)		0.7		mA
	Standby Mode (XOSC on, CLK Gen. on)		2.5		mA
	PLL mode		13.5		mA
	RX Mode (FSK 4Mbps)		33		mA
	TX Mode (FSK, 15dBm output)		88		mA
Synthesizer block					
Crystal settling time*[2]			0.6		ms
Crystal frequency*[4]			16		MHz
Crystal tolerance*[5]			±20		ppm
Crystal Load Capacitance			12		pF
Crystal ESR				40	ohm
PLL settling time*[6]	Standby to PLL		30		μs
Transmitter					
Carrier Frequency		5725		5850	MHZ
Maximum output power			15		dBm
Output power control range			20		dB
Out Band Spurious Emission	30MHz~1GHz			-36	dBm
	1GHz~12.75GHz			-30	dBm
	1.8GHz~ 1.9GHz			-47	dBm
Frequency deviation	Data rate 4Mbps		±1M		Hz
Data rate	FSK	0.5	2	4	Mbps
TX settling time	PLL to TX		60		μs
Receiver					
Receiver sensitivity@ BER = 0.1% (FSK)	4Mbps		-91		dBm
	2Mbps		-93		dBm
IF Filter bandwidth	4Mbps		5M		Hz
	2Mbps		2.5M		Hz
IF center frequency	4Mbps		4M		Hz
	2Mbps		2M		Hz
Interference*[3] (FSK)	Co-Channel (C/I_0)		11		dB
	±1 Adjacent Channel		4		dB
	±2 Adjacent Channel		- 18		dB
	±3 Adjacent Channel		- 28		dB
	±4 Adjacent Channel		- 32		dB
	Image (C/I_{IM})		- 12		dB
Maximum Operating Input Power	@RF input (BER=0.1%)			3	dBm
RX Spurious Emission	30MHz~1GHz			-57	dBm
	1GHz~12.75GHz			-47	
RSSI Range	AGC = on	-95		-20	dBm

	AGC = off	-95		-55	dBm
RX settling time	PLL to RX		60		µs
Regulator					
Regulator settling time			0.2		ms
Band-gap reference voltage			1.2		V
Regulator output voltage			1.2		V
Digital IO DC characteristics					
High Level Input Voltage (V_{IH})		0.8*VDD		VDD	V
Low Level Input Voltage (V_{IL})		0		0.2*VDD	V
High Level Output Voltage (V_{OH})	@I_{OH}= -0.5mA	VDD-0.4		VDD	V
Source current	@VOH = 2.4V		10		mA
Low Level Output Voltage (V_{OL})	@I_{OL}= 0.5mA	0		0.4	V
Sink current	@VOL = 0.4V		5		mA

Note 1: When digital I/O pin is configured as input, it will be pulled high internally.
Note 2: Xtal settling time depends on Xtal package type, Xtal ESR and Xtal Cm.
Note 3: The wanted signal is set above sensitivity level +3dB. The modulation data of wanted signal and interferer are PN9 and PN15, respectively. Channel spacing is one IF frequency.
Note 4: A5133 also supports 16.384 MHz crystal and the data rate will be multiplied by 1.024.
Note 5: For low data rate application, crystal tolerance should be tightened. Please contact AMICCOM's FAE.
Note 6: PLL settling time depends on loop bandwidth.

9. Control Register

A5133 has totally built-in 64 control registers that cover all radio control. MCU can access those control registers via 3-wire or 4-wire SPI (Support max. SPI data rate up to 10 Mbps). User can refer to chapter 10 for details of SPI interface. A5133 is simply controlled by registers and outputs its status to MCU by GIO1 and GIO2 pins.

9.1 Control Register Table

Address / Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h Mode	W	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN
	R	HECF	FECF	CRCF	CER	XER	PLLER	TRSR	TRER
01h Mode control	W	DDPC	ARSSI	AIF	DFCD	WORE	FMT	FMS	ADCM
	R	DDPC	ARSSI	AIF	CD	WORE	FMT	FMS	ADCM
02h Calc	R/W	XRCC	ADCC	RCC	VCC	VBC	VDC	FBC	RSSC
03h FIFO I	W	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
	R	LENF7	LENF6	LENF5	LENF4	LENF3	LENF2	LENF1	LENF0
04h FIFO II	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0
	R	FIFOPT7	FIFOPT6	FIFOPT5	FIFOPT4	FIFOPT3	FIFOPT2	FIFOPT1	FIFOPT0
05h FIFO Data	R/W	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
06h ID Data	R/W	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
07h RC OSC I	W	WOR_SL7	WOR_SL6	WOR_SL5	WOR_SL4	WOR_SL3	WOR_SL2	WOR_SL1	WOR_SL0
08h RC OSC II	W	WOR_SL9	WOR_SL8	WOR_AC 5	WOR_AC 4	WOR_AC 3	WOR_AC 2	WOR_AC 1	WOR_AC 0
09h RC OSC III	W	--	IRCHC	MRC	RCKS1	RCKS0	RCOSC_E	TSEL	TWOR_E
0Ah CKO Pin	W	ECKOE	CKOS3	CKOS2	CKOS1	CKOS0	CKOI	CKOE	SCKI
0Bh GIO1 Pin I	W	VKM	VPM	GIO1S3	GIOS2	GIO1S1	GIO1S0	GIO1I	GIO1OE
0Ch GIO2 Pin II	W	BBCKS1	BBCKS0	GIO2S3	GIO2S2	GIO2S1	GIO2S0	GIO2I	GIO2OE
0Dh Data Rate Clock	W	CGC1	CGC0	GRC3	GRC2	GRC1	GRC0	CGS	XS
	R	IFS1	IFS0	GRC3	GRC2	GRC1	GRC0	--	-
0Eh PLL I	R/W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
0Fh PLL II	W	--	RRC1	RRC0					IP8
	R	--	RRC1	RRC0					BIP8
10h PLL III	W	BIP7	BIP6	BIP5	BIP4	BIP3	BIP2	BIP1	BIP0
	R	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
11h PLL IV	W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8
	R	RAC15	RAC14	RAC13	RAC12	RAC11	RAC10	RAC9	RAC8
12h PLL V	W	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0
	R	RAC7	RAC6	RAC5	RAC4	RAC3	RAC2	RAC1	RAC0
13h Channel Group I	R/W	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
14h Channel Group II	R/W	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0
15h TX I	W	GDR	GF	TMDE	TXDI	TME	FDP2	FDP1	FDP0
16h TX II	W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
17h Delay I	W	TDL4	TDL3	TDL2	TDL1	TDL0	PDL2	PDL1	PDL0

18h Delay II	W	WSEL2	WSEL1	WSEL0	RSSC_D1	RSSC_D0	RS_DLY2	RS_DLY1	RS_DLY0
19h RX	W	MAGC	AGCE	RXSM1	RXSM0	AFC	RXDI	DMG	ULS
1Ah RX Gain I	R/W	--	IGC1	IGC0	MGC1	MGC0	--	LGC1	LGC0
1Bh RX Gain II	W	RSAGC1	RSAGC0	VTL2	VTL1	VTL0	VTH2	VTH1	VTH0
	R	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0
1Ch RX Gain III	W	RDU	IFS2	IFS1	IFS0	RSM1	RSM0	ERSSM	RSS
	R	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
1Dh RX Gain IV	W	LIMC	IFBC1	IFBC0	IFAS	MHC1	MHC0	LHC1	LHC0
1Eh RSSI Threshold	W	RTH7	RTH6	RTH5	RTH4	RTH3	RTH2	RTH1	RTH0
	R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
1Fh ADC Control	W	AVSEL1	AVSEL0	MVSEL1	MVSEL0	RADC	FSARS	XADS	CDM
	R	SNF7	SNF6	SNF5	SNF4	SNF3	SNF2	SNF1	SNF0
20h Code I_P0	W	--	WHTS	FECS	CRCS	IDL1	IDL0	EPML1	EPML0
	R	SNF15	SNF14	SNF13	SNF12	SNF11	SNF10	SNF9	SNF8
20h DSSS4_P4	W								DSSS
	R								
21h Code II_P0	W	MSCRC	EDRL	HECS	ETH2	ETH1	ETH0	PTH1	PTH0
	R	MTCRCF7	MTCRCF6	MTCRCF5	MTCRCF4	MTCRCF3	MTCRCF2	MTCRCF1	MTCRCF0
21h EXT1_P6		PDNPAS	VRPL[2]	VRPL[1]	VRPL[0]	VBPAS_BF	VBPAS	TXLB[1]	TXLB[0]
21h EXT2_P8			TPA[2]	TPA[1]	TPA[0]	SWM	RFINE[2]	RFINE[1]	RFINE[0]
21h EXT3_P9		PORIPS	PMPAR	PM1SWE	PM1SW[1]	PM1SW[0]	PGV_PA[2]	PGV_PA[1]	PGV_PA[0]
21h EXT4_P10		IGM[3]	IGM[2]	IGM[1]	IGM[0]	ICONTROL[1]	ICONTROL[0]	IBPAS	ENRC
21h EXT5_P11		KICS[1]	KICS[0]	CPM[1]	CPM[0]	CI[1]	CI[0]	CBBF[1]	CBBF[0]
21h EXT6_P12		CSXTL[7]	CSXTL[6]	CSXTL[5]	CSXTL[4]	CSXTL[3]	CSXTL[2]	CSXTL[1]	CSXTL[0]
22h Code III_P0	W	CRCINV	WS6	WS5	WS4	WS3	WS2	WS1	WS0
	R	MTCRCF15	MTCRCF14	MTCRCF13	MTCRCF12	MTCRCF11	MTCRCF10	MTCRCF9	MTCRCF8
22h EXT7_P1	W	TXHP	BGCS	BIAS	TXLPN	PSDPAS[2]	PSDPAS[1]	PSDPAS[0]	XRCS
22h EXT8_P2	W	MTRIM7	MTRIM6	MTRIM5	MTRIM4	MTRIM3	MTRIM2	MTRIM1	MTRIM0
	R	TRIM7	TRIM6	TRIM5	TRIM4	TRIM3	TRIM2	TRIM1	TRIM0
22h EXT9_P3	W	PGV_P1	PGV_P0	EKIC_SEL1	EKIC_SEL0	--	--	--	MTRIM8
	R								TRIM8
22h EXT10_P4	W	TGNUM1_7	TGNUM1_6	TGNUM1_5	TGNUM1_4	TGNUM1_3	TGNUM1_2	TGNUM1_1	TGNUM1_0
	R	NUMLH1_7	NUMLH1_6	NUMLH1_5	NUMLH1_4	NUMLH1_3	NUMLH1_2	NUMLH1_1	NUMLH1_0
22h EXT11_P5	W	--	REGCL_PA	MVS1_1	MVS1_0	MXRC	TGNUM1_10	TGNUM1_9	TGNUM1_8
	R						NUMLH1_10	NUMLH1_9	NUMLH1_8
23h IF Calibration I	W	HFR	CKGS1	CKGS0	MFBS	MFB3	MFB2	MFB1	MFB0
	R	-	-	-	FBCF	FB3	FB2	FB1	FB0

24h IF Calibration II	W	PDNTXS	RAMPS2	RAMPS1	RAMPS0	DTDS3	DTDS2	DTDS1	DTDS0
	R	--	--	--	FCD4	FCD3	FCD2	FCD1	FCD0
25h VCO current Calibration	W	CSW	DEVCM	VCRLS	MVCS	VCOC3	VCOC2	VCOC1	VCOC0
	R	-	-	-	VCCF	VCB3	VCB2	VCB1	VCB0
26h VCO band Calibration I	W	DCD1	DCD0	DAGS	MVBS	MVB3	MVB2	MVB1	MVB0
	R	-	-	-	VBCF	VB3	VB2	VB1	VB0
27h VCO band Calibration II	W	MDAG7	MDAG6	MDAG5	MDAG4	MDAG3	MDAG2	MDAG1	MDAG0
	R	ADAG7	ADAG6	ADAG5	ADAG4	ADAG3	ADAG2	ADAG1	ADAG0
28h VCO deviation Calibration I	W	DEVS3	DEVS2	DEVS1	DEVS0	DAMR_M	VMTE_M	VMS_M	MSEL
	R	DEVA7	DEVA6	DEVA5	DEVA4	DEVA3	DEVA2	DEVA1	DEVA0
29h VCO deviation Calibration II	W	MVDS	DEVM6	DEVM5	DEVM4	DEVM3	DEVM2	DEVM1	DEVM0
	R	DEVC7	DEVC6	DEVC5	DEVC4	DEVC3	DEVC2	DEVC1	DEVC0
2Ah DAS_P0	W	QLIM	PRS						FBOP
2Ah DAS_P1	W	RFBS	CKGU	IFTS	TRDC	LNAVR			INTPRC
2Ah DAS_P2	W	VTRB3	VTRB2	VTRB1	VTRB0	VMRB3	VMRB2	VMRB1	VMRB0
2Ah DAS_P3	W	DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0
2Ah DAS_P4	W	VMG7	VMG6	VMG5	VMG4	VMG3	VMG2	VMG1	VMG0
	R	VMG7	VMG6	VMG5	VMG4	VMG3	VMG2	VMG1	VMG0
2Ah DAS_P5		--	PKTH	PKT1	PKT0	PKS	PKIS1	PKIS0	IFPK
2Ah DAS_P6		--	HPLS			LOVRS	TXLO_HC	PAB_HCS	PA_HCS
2Ah DAS_P7		XDS	VRSEL	MS	MSCL4	MSCL3	MCSL2	MCSL1	MSCL0
2Ah DAS_P8	W	MRCT7	MRCT6	MRCT5	MRCT4	MRCT3	MRCT2	MRCT1	MRCT0
	R	RCT7	RCT6	RCT5	RCT4	RCT3	RCT2	RCT1	RCT0
2Ah DAS_P9	W	TGNUM11	TGNUM10	TGNUM9	TGNUM8	MVS1	MVS0	MRCT9	MRCT8
	R	NUMLH11	NUMLH10	NUMLH9	NUMLH8	--	--	RCT9	RCT8
2Ah DAS_P10	W	TGNUM7	TGNUM6	TGNUM5	TGNUM4	TGNUM3	TGNUM2	TGNUM1	TGNUM0
	R	NUMLH7	NUMLH6	NUMLH5	NUMLH4	NUMLH3	NUMLH2	NUMLH1	NUMLH0
2Ah DAS_P11	W	RCOT2	RCOT1	RCOT0					
2Ah DAS_P12		MTCRCS	DRS	SPL1	SPL0	--	--	--	--
2Bh VCO modulation Delay	W	DMV1	DMV0	DEVFD2	DEVFD1	DEVFD0	DEVD2	DEVD1	DEVD0
2Ch Battery detect	W		PM1S	BGS	QDS	BVT2	BVT1	BVT0	BD_E
	R	--			BDF	BVT2	BVT1	BVT0	BD_E
2Dh TX test	W	ASMV1	ASMV0	TXCS			TBF2	TBF1	TBF0
2Eh Rx DEM test I	W	DMT	DCM1	DCM0	CDPM	MXT	SLF2	SLF1	SLF0
2Fh Rx DEM test II	W	AGCH1	AGCH0	DCL2	DCL1	DCL0	RAW	--	MOVS

30h Charge Pump Current I	W	CPM3	CPM2	CPM1	CPM0	CPT3	CPT2	CPT1	CPT0
31h Charge Pump Current II	W	CPTX3	CPTX2	CPTX1	CPTX0	CPRX3	CPRX2	CPRX1	CPRX0
32h Crystal test	W	--	CPS	CPCH1	CPCH0	CPCS	XCC	XCP1	XCP0
33h PLL test	W	MDEN		PRIC1	PRIC0	PRRC1	PRRC0	SDPW	NSDO
34h VCO test	W	DEVGD2	DEVGD1	DEVGD0	RLB1	RLB0	VBS2	VBS1	VBS0
35h RF Analog test	W	AGT3	AGT2	AGT1	AGT0	RFT3	RFT2	RFT1	RFT0
36h Key_data	W/R	KEY7	KEY6	KEY5	KEY4	KEY3	KEY2	KEY1	KEY0
37h Channel Select	W	CHI3	CHI2	CHI1	CHI0	CHD3	CHD2	CHD1	CHD0
38h ROM_P0	W	BDC5	BDC4	BDC3	BDC2	BDC1	BDC0	REGCL	PD_BOD
38h ROM_P1	W	--	REGVS	--	FBG4	FBG3	FBG2	FBG1	FBG0
	R	--	--	--	FBGR4	FBGR3	FBGR2	FBGR1	FBGR0
38h ROM_P2	W	--	--	CTR5	CTR4	CTR3	CTR2	CTR1	CTR0
	R	--	--	CTRR5	CTRR4	CTRR3	CTRR2	CTRR1	CTRR0
38h ROM_P3	W	FGC1	FGC0	SRS2	SRS1	SRS0	CRS2	CRS1	CRS0
	R	--	--	SRSR2	SRSR1	SRSR0	CRSR2	CRSR1	CRSR0
38h ROM_P4	W	--	STMP	STM5	STM4	STM3	STM2	STM1	STM0
	R	--	STMP	STMR5	STMR4	STMR3	STMR2	STMR1	STMR0
38h ROM_P5		CDPS	CDPN	PMPN	--	DEVSUB	FPS2	FPS1	FPS0
38h ROM_P6		TGM7	TGM6	TGM5	TGM4	TGM3	TGM2	TGM1	TGM0
38h ROM_P7		DVO15	DVO14	DVO13	DVO12	DVO11	DVO10	DVO9	DVO8
38h ROM_P8		DVO7	DVO6	DVO5	DVO4	DVO3	DVO2	DVO1	DVO0
38h ROM_P9	W	EFSW	EFWE	EFRE			EFB2	EFB1	EFB0
38h ROM_P10	W		PSDS2	PSDS1	PSDS0	PDNFH	QDSFH	PDNFL	QDSFL
38h ROM_P11	W							CBIST	BIST
	R	BER7	BER6	BER5	BER4	BER3	BER2	BER1	BER0
39h Data Rate CLK	W	SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
3Ah FCR	W	FCL1	FCL0	ARC3	ARC2	ARC1	ARC0	EACKS	EARTS
	R	ARTEF	VPOAK	RCR3	RCR2	RCR1	RCR0	EACKS	EARTS
3Bh ARD	W	ARD7	ARD6	ARD5	ARD4	ARD3	ARD2	ARD1	ARD0
3Ch AFEP	W	EACKF	SPSS	ACKFEP5	ACKFEP4	ACKFEP3	ACKFEP2	ACKFEP1	ACKFEP0
	R	--	--	EARTS	EARTS	EARTS	TXSN2	TXSN1	TXSN0
3Dh FCB	W/R	FCB7	FCB6	FCB5	FCB4	FCB3	FCB2	FCB1	FCB0
3Eh KEYCl	W	KEYOS	AFIDS	ARTMS	MIDS	AESS	--	AKFS	EDCRS
3Fh ID code	W	RND7	RND6	RND5	RND4	RND3	RND2	RND1	RND0
	R	ICD7	ICD6	ICD5	ICD4	ICD3	ICD2	ICD1	ICD0

Legend: - = unimplemented

9.2 Control Register Description

9.2.1 Mode Register (Address: 00h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN
R	HECF	FECF	CRCF	CER	XER	PLLER	TRSR	TRER
Reset	--	--	--	--	--	--	--	--

RESETN: Write to this register by 0x00 to issue reset command, then it is auto clear

HECF: Head Control Flag. (Clear by any Strobe command.)
HEC is CRC-8 result from FCB + DFL.
[0]: HEC pass.
[1]: HEC error.

FECF: FEC flag. (FECF is read clear.)
[0]: FEC pass.
[1]: FEC error.

CRCF: CRC flag. (CRCF is read clear.)
[0]: CRC pass.
[1]: CRC error.

CER: RF chip enable Register.
[0]: RF chip is disabled.
[1]: RF chip is enabled.

XER: Internal crystal oscillator enable Register.
[0]: Crystal oscillator is disabled.
[1]: Crystal oscillator is enabled.

PLLER: PLL enable Register.
[0]: PLL is disabled.
[1]: PLL is enabled.

TRSR: TRX Mode Select Register.
[0]: RX.
[1]: TX. When TRE set, the chip will enter TX or RX mode by TRS register.

TRER: TRX Enable Register.
[0]: Disable.
[1]: Enable. It will be clear after end of packet encountered in FIFO mode.

9.2.2 Mode Control Register (Address: 01h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	DDPC	ARSSI	AIF	DFCD	WORE	FMT	FMS	ADCM
R	DDPC	ARSSI	AIF	CD	WORE	FMT	FMS	ADCM
Reset	0	0	0	0	0	0	0	0

DDPC (Direct mode data pin control): Direct mode modem data can be accessed via SDIO pin when this register is enabled.
[0]: Disable.
[1]: Enable.

ARSSI: Auto RSSI measurement while entering RX mode. Recommend ARSSI = [1].
[0]: Disable.
[1]: Enable.

AIF (Auto IF Offset): RF LO frequency will auto offset one IF frequency while entering RX mode.
[0]: Disable.
[1]: Enable.
If AIF =1, then,
$F_{RXLO} = F_{PLLS} - F_{IF}$, for up side band (ULS = 0, 19h).
$F_{RXLO} = F_{PLLS} + F_{IF}$, for low side band (ULS = 1, 19h)

CD / DFCD: DFCD: Data Filter by CD.
[0]: Disable.

[1]: Enable. The data package would be filtered while the input power level is below the threshold level (RTH[7:0], 1Eh).

DFCD (Read only): Carrier detector signal.
[0]: Input power below threshold.
[1]: Input power above threshold.

WORE: Wake On RX enable.
[0]: Disable.
[1]: Enable.

FMT: Reserved for internal usage only.

FMS: Direct/FIFO mode select.
[0]: Direct mode.
[1]: FIFO mode.

ADCM: ADC measurement enables (Auto clear when done).
[0]: Disable measurement or measurement finished.
[1]: Enable measurement.

ADCM	A5133 @ Standby mode	A5133 @ RX mode
[0]	Disable ADC	Disable ADC
[1]	Measure temperature	Measure RSSI, carrier detect

9.2.3 Calibration Control Register (Address: 02h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	XRCC	ADCC	RCC	VCC	VBC	VDC	FBC	RSSC
R	XRCC	ADCC	RCC	VCC	VBC	VDC	FBC	RSSC
Reset	0	0	0	0	0	0	0	0

XRCC: 16M XRC calibration enable (Auto clear when done).
[0]: Disable.
[1]: Enable.

ADCC: ADC calibration enable (Auto clear when done).
[0]: Disable.
[1]: Enable.

RCC: RC Oscillator calibration enable (Auto clear when done).
[0]: Disable.
[1]: Enable.

VCC: VCO Current calibration enable (Auto clear when done).
[0]: Disable.
[1]: Enable .

VBC: VCO Bank calibration enable (Auto clear when done).
[0]: Disable.
[1]: Enable.

VDC: VCO Deviation calibration enable (Auto clear when done).
[0]: Disable.
[1]: Enable.

FBC: IF Filter Bank calibration enable (Auto clear when done).
[0]: Disable .
[1]: Enable.

RSSC: RSSI calibration enable (Auto clear when done).
[0]: Disable.
[1]: Enable.

9.2.4 FIFO Register I (Address: 03h)

R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W	--	--	--	--	FEP11	FEP10	FEP9	FEP8
R	--	--	--	--	LENF11	LENF10	LENF9	LENF8
Reset	--	--	--	--	0	0	0	0
R/W	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
W	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
R	LENF7	LENF6	LENF5	LENF4	LENF3	LENF2	LENF1	LENF0
Reset	0	0	0	0	0	0	0	0

FEP [11:0]: FIFO End Pointer for TX FIFO and Rx FIFO.
FIFO length = (FEP+1) bytes.

LENF [11:0]: Received FIFO Length = LENF + 1.
Used in dynamic length mode. (EDRL = 1).

9.2.5 FIFO Register II (Address: 04h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0
R	FIFOPT7	FIFOPT6	FIFOPT5	FIFOPT4	FIFOPT3	FIFOPT2	FIFOPT1	FIFOPT0
Reset	0	1	0	0	0	0	0	0

FPM [1:0]: FIFO Pointer Margin
[00]: 4 bytes.
[01]: 8 bytes.
[10]: 12 bytes.
[11]: 16 bytes.

PSA [5:0]: Used for Segment FIFO.

FIFOPT[7:0]: FIFO pointer index (read only).
The FIFO access pointer = FIFOPT x 2.

9.2.6 FIFO DATA Register II (Address: 05h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
R	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
Reset	0	0	0	0	0	0	0	0

FIFO [7:0]: FIFO data.
TX FIFO and RX FIFO share the same address (05h).
TX FIFO is max 64-byte write only.
RX FIFO is max 64-byte read only.

9.2.7 ID DATA Register (Address: 06h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Reset	0	0	0	0	0	0	0	0

ID [7:0]: ID data (sync word, max 8 bytes).
When this address is accessed, ID Data is input or output sequential (ID Byte 0,1, 2, 3 …., 7) corresponding to Write or Read.

9.2.8 RC OSC Register I (Address: 07h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	WOR_SL7	WOR_SL6	WOR_SL5	WOR_SL4	WOR_SL3	WOR_SL2	WOR_SL1	WOR_SL0
R								
Reset	0	0	0	0	0	0	0	0

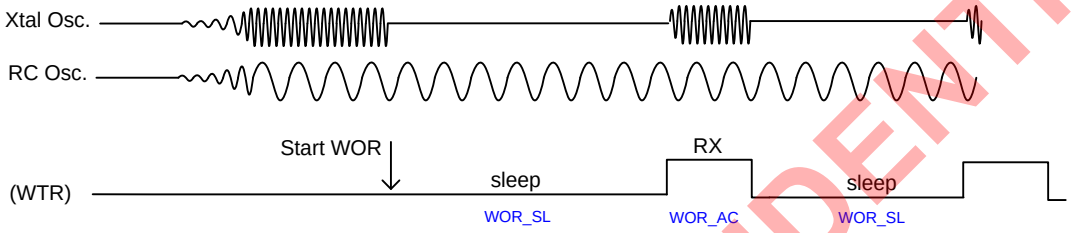
9.2.9 RC OSC Register II (Address: 08h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	WOR_SL9	WOR_SL8	WOR_AC5	WOR_AC4	WOR_AC3	WOR_AC2	WOR_AC1	WOR_AC0
R								
Reset	0	0	0	0	0	0	1	1

WOR_AC [5:0]: 6-bits WOR Active Timer for TWOR Function

WOR_SL [9:0]: 10-bits WOR Sleep Timer for TWOR Function.
WOR_SL [9:0] are from address (07h) and (08h),

Device Active = (WOR_AC+1) x (1/4000), (250us ~ 16ms).
Device Sleep = (WOR_SL+1) x (1/4000) x 32, (8ms ~ 8.192s).



9.2.10 RC OSC Register III (Address: 09h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--	IRCHC	MRC	RCKS1	RCKS0	RCOSC_E	TSEL	TWOR_E
R								
Reset	--	0	0	1	1	0	0	0

IRCHC: Ring oscillator high current mode select.

MRC: Manual RC Bank value setting.
[0]: Auto.
[1]: Manual.

RCKS [1:0]: RO calibration clock select:
[00]: 32XDR
[01]: 16MHz
[1x]: 8XDR

RCOSC_E: RC Oscillator Enable.
[0]: Disable.
[1]: Enable.

TSEL: Timer select for TWOR function.
[0]: Use WOR_AC.
[1]: Use WOR_SL.

TWOR_E: Enable TWOR function.
[0]: Disable TWOR function.
[1]: Enable TWOR mode. Wake up MCU by a periodic TWOR output.

9.2.11 CKO Pin Control Register (Address: 0Ah)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	ECKOE	CKOS3	CKOS2	CKOS1	CKOS0	CKOI	CKOE	SCKI
R								
Reset	1	0	1	1	1	0	1	0

ECKOE: External Clock Output Enable for CKOS [3:0]= [0100] ~ [0111].
[0]: Disable.
[1]: Enable.

CKOS [3:0]: CKO pin output select.

[0000]: DCK (TX data clock).
[0001]: RCK (RX recovery clock).
[0010]: FPF (FIFO pointer flag).
[0011]: Logic OR gate by EOP, EOVBC, EOFBC, EOVCC, EOVDC, RSSC_OK and inverter signal of X'tal ready. (Internal usage only).
[0100]: F_{SYCK} / 2.
[0101]: F_{SYCK} / 4.
[0110]: RXD.
[0111]: BOD.
[1000]: WCK.
[1001]: FSYNC.
[1010]: ROSC.
[1011]: MXDEC (MXT=0:inverter signal of OKADCN, MXT=1: DEC)
[1100]: BDF.
[1101]: F_{SYCK} .
[1110]: VPOAK
[1111]: WRTC.

CKOI: CKO pin output signal invert.
[0]: Non-inverted output.
[1]: Inverted output.

CKOE: CKO pin Output Enable.
[0]: High Z.
[1]: Enable.

SCKI: SPI clock input invert.
[0]: Non-inverted input.
[1]: Inverted input.

9.2.12 GIO1 Pin Control Register (Address: 0Bh)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	VKM	VPM	GIO1S3	GIO1S2	GIO1S1	GIO1S0	GIO1I	GIO1OE
R								
Reset	0	0	0	0	0	0	0	1

VKM: Valid packet mode select.
[0]: by event.
[1]: by pulse.

VPM: Valid Pulse width select.
[0]: 10us.
[1]: 30us.

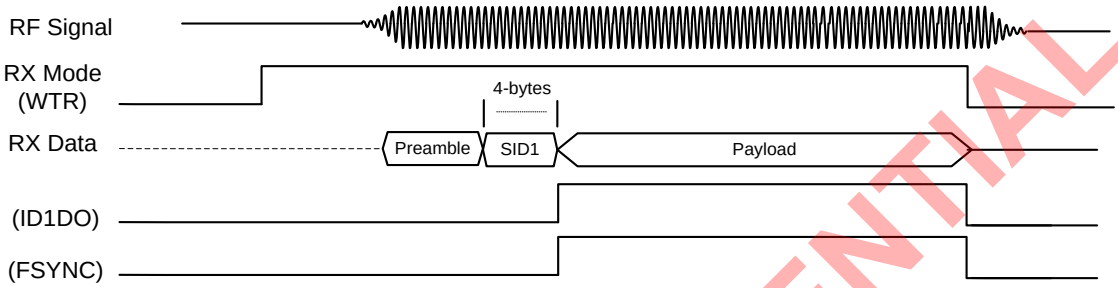
GIO1S [3:0]: GIO1 pin function select.

GIO1S [3:0]	TX state	RX state
[0000]	WTR (Wait until TX or RX finished)	
[0001]	EOAC (end of access code)	FSYNC
[0010]	TMEO or TMDEO(TX modulation enable)	CD(carrier detect)
[0011]	SID1 Detect Output(ID1DO)	
[0100]	RCOSC_E=1: MCU wakeup signal (TWOR); RCOSC_E=0: CWTR	
[0101]	MTCRCINT / VTB0 /In phase demodulator input(DMII)	
[0110]	SDO (4 wires SPI data out)	
[0111]	TRXD In/Out (Direct mode)	
[1000]	RXD (Direct mode)	
[1001]	TXD (Direct mode)	
[1010]	PDN_RX	
[1011]	External FSYNC input in RX direct mode *	
[1100]	MXINC(MXT=0:EOADC.MXT=1:INC.)	
[1101]	FPF	

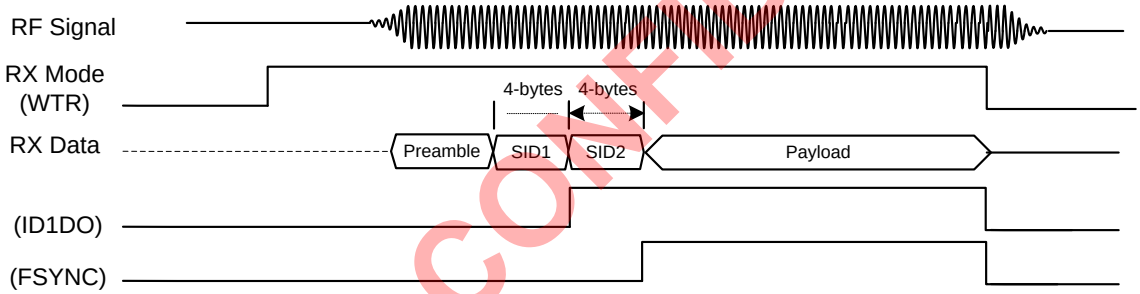
[1110]	VPOAK (Auto Resend OK Output)
[1111]	FMTDO (FIFO mode TX Data Output testing)

If GIO1S=[1011] and direct mode is selected, the internal frame sync function will be disabled. In such case, it is recommended that user asserts frame sync signal to this input to get better DC estimation of demodulation.

<Case 1: If IDL = [01], ID = 4-bytes>



<Case 2: If IDL = [11], ID = 8-bytes>



GIO1I: GIO1 pin output signal invert.
[0]: Non-inverted output.
[1]: Inverted output.

GIO1OE: GIO1pin output enable.
[0]: High Z.
[1]: Enable.

9.2.13 GIO2 Pin Control Register (Address: 0Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	BBCKS1	BBCKS0	GIO2S3	GIO2S2	GIO2S1	GIO2S0	GIO2I	GIO2OE
R								
Reset	0	1	0	1	0	0	0	1

BBCKS [1:0]: Clock select for digital block.
[00]: F_{SYCK}
[01]: F_{SYCK} / 2.
[10]: F_{SYCK} / 4.
[11]: F_{SYCK} / 8.
F_{SYCK} is A5133's System clock = 16MHz.

GIO2S [3:0]: GIO2 pin function select.

GIO2S [3:0]	TX state	RX state
[0000]	WTR (Wait until TX or RX finished)	
[0001]	EOAC (end of access code)	FSYNC(frame sync)
[0010]	TMEO(TX modulation enable)	CD(carrier detect)
[0011]	SID1 Detect Output (ID1DO	

[0100]	RCOSC_E=1: MCU wakeup signal (TWOR); RCOSC_E=0: CWTR
[0101]	MTCRCINT/ VTB1 /Quadrature phase demodulator output (DMIQ).
[0110]	SDO (4 wires SPI data out)
[0111]	TRXD In/Out (Direct mode)
[1000]	RXD (Direct mode)
[1001]	TXD (Direct mode)
[1010]	PDN_TX
[1011]	
[1100]	BDF
[1101]	FPF
[1110]	VPOAK (Auto Resend OK Output)
[1111]	FMTCK (FIFO mode TX Data clock Output testing)

GIO2I: GIO2 pin output signal invert.
[0]: Non-inverted output.
[1]: Inverted output.

GIO2OE: GIO1pin output enable.
[0]: High Z.
[1]: Enable.

9.2.14 Data Rate Clock Register (Address: 0Dh)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CGC1	CGC0	GRC3	GRC2	GRC1	GRC0	CGS	XS
R	IFS1	IFS0	GRC3	GRC2	GRC1	GRC0	--	--
Reset	0	0	0	1	1	1	1	1

CGC[1:0]: Clock generation current setting.

GRC [3:0]: Generator Reference Counter.
Clock generation reference = $F_{CRYSTAL}$ / (GRC+1). Maximum divide ratio is 16.

CGS: Clock generator enable.
[0]: Disable.
[1]: Enable.

XS: Crystal oscillator select. Recommend XS = [1].
[0]: Use external clock.
[1]: Use external crystal.

9.2.15 PLL Register I (Address: 0Eh)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
R	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
Reset	0	1	0	1	0	1	0	0

CHN [7:0]: RF LO Channel number.

9.2.16 PLL Register II (Address: 0Fh)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--	RRC1	RRC0					BIP8
R	--	RRC1	RRC0					IP8
Reset	--	0	0					0

RRC [1:0]: RF PLL reference counter setting.
The PLL comparison frequency, $F_{PFD} = F_{CRYSTAL}$ / (RRC+1).

9.2.17 PLL Register III (Address: 10h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	BIP7	BIP6	BIP5	BIP4	BIP3	BIP2	BIP1	BIP0
R	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0

Reset	1	0	0	1	0	1	1	0

BIP [8:0]: (write) LO base frequency integer part setting.
BIP [8:0] are from address (0Fh) and (10h),

IP [8:0]: (read) LO frequency integer part value.
IP [8:0] are from address (0Fh) and (10h),

9.2.18 PLL Register IV (Address: 11h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8
R	RAC15	RAC14	RAC13	RAC12	RAC11	RAC10	RAC9	RAC8
Reset	0	0	0	0	0	0	0	0

9.2.19 PLL Register V (Address: 12h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0
R	RAC7	RAC6	RAC5	RAC4	RAC3	RAC2	RAC1	RAC0
Reset	0	0	0	0	0	1	0	0

BFP [15:0]: LO base frequency fractional part setting. (BFP = [0000] is forbidden.)
BFP [15:0] are from address (11h) and (12h),

RAC [15:0] (Read): AFC frequency compensation value or Fractional part of PLL.
AC [14:0]: AFC frequency compensated value.
FP [15:0]: Fractional part of PLL.

AFC	RAC [15]	RAC [14:0]
0	FSYNC	AC [14:0]
1	FP [15]	FP [14:0]

9.2.20 Channel Group Register I (Address: 13h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
R	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
Reset	0	0	1	1	1	1	0	0

CHGL [7:0]: PLL channel group low boundary setting.

9.2.21 Channel Group Register II (Address: 14h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0
R	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0
Reset	0	1	1	1	1	0	0	0

CHGH [7:0]: PLL channel group high boundary setting.

PLL frequency is divided into 3 groups for calibration purpose:

	Channel
Group1	0 ~ CHGL-1
Group2	CHGL ~ CHGH-1
Group3	CHGH ~ 255

Note: Each group needs its own VCO current, bank and deviation calibration. Use the same calibration value for the frequency in the same group.

9.2.22 TX Register I (Address: 15h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	GDR	GF	TMDE	TXDI	TME	FDP2	FDP1	FDP0
R								

Reset	0	0	1	0	1	1	1	1

GDR: Gaussian Filter Over-sampling Rate Select. Recommend GDR = [0].

GF: Gaussian Filter Select.
[0]: Disable.
[1]: Enable.

TMDE: TX Modulation Enable for VCO Modulation. Recommend TMDE = [1].
[0]: Disable.
[1]: Enable.

TXDI: TX data invert. Recommend TXDI = [0].
[0]: Non-invert.
[1]: Invert.

TME: TX modulation enable. Recommend TME = [1].
[0]: Disable.
[1]: Enable.

FDP [2:0]: Frequency deviation power setting.

9.2.23 TX Register II (Address: 16h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
R								
Reset	0	1	0	0	0	0	0	0

FD [7:0]: TX Frequency Deviation setting.

Formula : $F_{DEV} = (F_{PFD} * 127 * (FD\ [7:0] + 1) * 2^{(FDP\ [2:0] + 1)} / 2^{25}) * 4$.

Data Rate	FDP[2:0]	FD[7:0]	Fdev (KHz)
4Mbps	101	0x40	1000
2Mbps	100	0x40	500

9.2.24 Delay Register I (Address: 17h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	TDL4	TDL3	TDL2	TDL1	TDL0	PDL2	PDL1	PDL0
R								
Reset	0	0	0	1	0	0	0	0

TDL [4:0]: Delay for TRX settling from WPLL to TX/RX.
Delay= 20 * (TDL [4:0]) us for TDL> 0; 8us for TDL= 0.

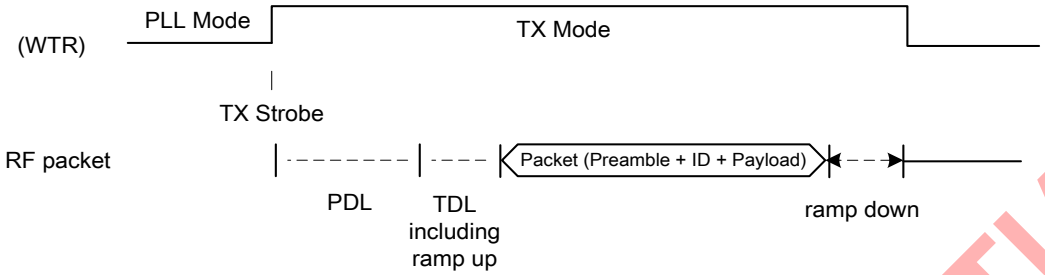
TDL [4:0]	WPLL to TX	Note
00000	8us	
00001	20 us	
00010	40 us	
00011	60 us	
…	…	…

TDL and ramp up start at the same time. TDL must be greater than ramp up time.
Ramp up time= 8 * ramp up clock period = $(8 * 2^{ASMV})$ us.
Ramp down time= $(8 * 2^{ASMV})$ + (8 * PDNTXS) us.

PDL [2:0]: Delay for TX settling from PLL to WPLL.
Delay= 20 * (PDL [2:0]) us.

PDL [2:0]	PLL to WPLL (LO freq changed)	Note
000	0 us	
001	20 us	

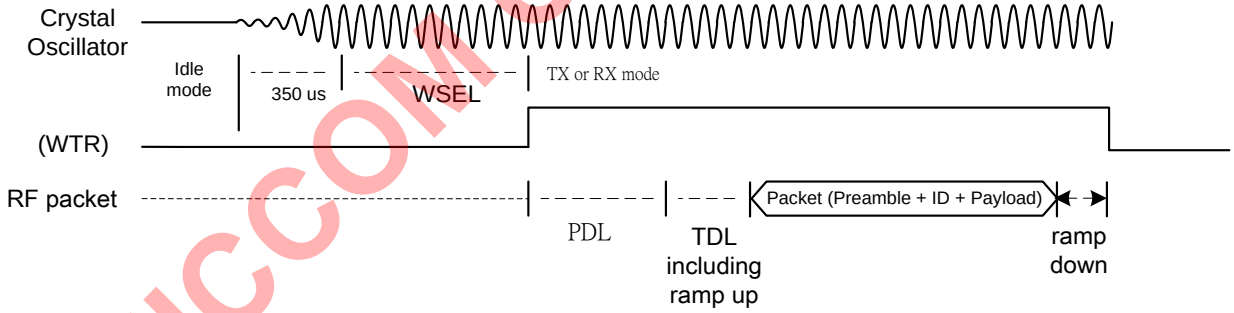
010	40 us	
011	60 us	
100	80 us	



9.2.25 Delay Register II (Address: 18h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	WSEL2	WSEL1	WSEL0	RSSC_D1	RSSC_D0	RS_DLY2	RS_DLY1	RS_DLY0
R								
Reset	0	1	0	0	0	0	0	1

WSEL [2:0]: XTAL settling delay setting (200us ~ 2.5ms).
[000]: 200us.
[001]: 400us.
[010]: 600us.
[011]: 800us.
[100]: 1ms.
[101]: 1.5ms.
[110]: 2ms.
[111]: 2.5ms.



RSSC_D [1:0]: RSSI calibration switching time (10us ~ 40us). Recommend RSSC_D = [00].
[00]: 10us.
[01]: 20us.
[10]: 30us.
[11]: 40us.

RS_DLY [2:0]: RSSI measurement delay (10us ~ 80us). Recommend RS_DLY = [000].
[000]: 10us.
[001]: 20us.
[010]: 30us.
[011]: 40us.
[100]: 50us.
[101]: 60us.
[110]: 70us.
[111]: 80us.

9.2.26 RX Register (Address: 19h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	MAGC	AGCE	RXSM1	RXSM0	AFC	RXDI	DMG	ULS
R								
Reset	0	1	1	0	0	0	0	0

MAGC: Manual AGC control. Recommend MAGC = [0].
[0]: auto gain control by AGCE,
[1]: manual gain control.

AGCE: Auto Front end Gain Control Select. Recommend AGCE = [1].
[0]: Disable.
[1]: Enable.

RXSM1: RX clock recovery circuit moving average filter length. Recommend RXSM1 = [1].
[0]: 4 bits.
[1]: 8 bits.

RXSM0: Demodulator LPF Bandwidth Select. Recommend RXSM0 = [1].
[0]: 2MHz.
[1]: 1MHz.

AFC: Auto Frequency compensation.
[0]: Disable.
[1]: Enable.

RXDI: RX data output invert. Recommend RXDI = [0].
[0]: Non-inverted output.
[1]: Inverted output.

DMG: Demodulator Gain Select. Recommend DMG = [0].
[0]: x 1.
[1]: x 3.

ULS: RX Up/Low side band select. Recommend ULS = [0].
[0]: Up side band,
[1]: Low side band.

9.2.27 RX Gain Register I (Address: 1Ah)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--	IGC1	IGC0	MGC1	MGC0	--	LGC1	LGC0
R	--	IGC1	IGC0	MGC1	MGC0	--	LGC1	LGC0
Reset	--	1	1	1	1	--	1	1

IGC [1:0]: IFA Attenuation Select.
[00]: -12dB.
[01]: -6dB.
[10]: -2dB.
[11]: -0dB.

MGC [1:0]: Mixer Gain Attenuation select.
[00]: -18dB.
[01]: -12dB.
[10]: -6dB.
[11]: 0dB.

LGC [1:0]: LNA Gain Attenuation select.
[00]: -18dB.
[01]: -12dB.
[10]: -6dB.
[11]: 0dB.

9.2.28 RX Gain Register II (Address: 1Bh)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RSAGC1	RSAGC0	VTL2	VTL1	VTL0	VTH2	VTH1	VTH0
R	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0
Reset	1	1	0	0	1	0	0	1

RSAGC [1:0]: AGC clock select. Recommend RSAGC = [11].
[00]: $8*F_{IF}$.
[01]: $4*F_{IF}$.
[10]: $2*F_{IF}$.
[11]: F_{IF}.

VTH [2:0] (write): auto gain control high voltage threshold select.

VTL [2:0] (write): auto gain control low voltage threshold select.

RH [7:0]: RSSI Calibration High Threshold (read only).

9.2.29 RX Gain Register III (Address: 1Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RDU	IFS2	IFS1	IFS0	RSM1	RSM0	ERSSM	RSS
R	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
Reset	1	0	1	1	1	1	0	0

RDU: Reserved for internal use.

IFS [2:0]: IF Frequency Select.
[000]: 1MHz.
[001]: 2MHz.
[010]: 3MHz.
[011]:4MHz.
[Others]: Reserved.

RSM [1:0]: RSSI Margin = RTH – RTL.
[00]: 5.
[01]: 10.
[10]: 15.
[11]: 20.

ERSSM: Ending Mode Select in RSSI Measurement.
[0]: RSSI ending by leaving RX.
[1]: RSSI ending by Frame SYNC.

RSS: RSSI measurement select.
[0]: Disable.
[1]: Enable.

RL [7:0]: RSSI Calibration Low Threshold (read only).

9.2.30 RX Gain Register IV (Address: 1Dh)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	LIMC	IFBC1	IFBC0	IFAS	MHC1	MHC0	LHC1	LHC0
R								
Reset	1	1	0	0	1	0	1	0

LIMC: IF limiter current select.
[0]: 0.3mA.
[1]: 0.6mA.

IFBC [1:0]: IF BPF current Select.

IFAS: IF amplifier current setting.

MHC [1:0]: Mixer Current Select.
[00]: 0.9 mA..
[01]: 1.2 mA.
[10]: 1.5 mA.
[11]: 1.8 mA.

LHC[1:0]: LNA Current Select.
[00]: 1mA.
[01]: 2mA.
[10]: 3mA.
[11]: 4mA.

9.2.31 RSSI Threshold Register (Address: 1Eh)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RTH7	RTH6	RTH5	RTH4	RTH3	RTH2	RTH1	RTH0
R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
Reset	0	0	0	0	0	0	0	0

ADC [7:0]: ADC output value of thermal sensor and RSSI (read only).
ADC input voltage= 0.6 * ADC [7:0] / 256 V.

RTH [7:0]: Carrier detect threshold.
CD (Carrier Detect) =1 when RSSI ≧ RTH.
CD (Carrier Detect) =0 when RSSI < RTL.

9.2.32 ADC Control Register (Address: 1Fh)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	AVSEL1	AVSEL0	MVSEL1	MVSEL0	RADC	FSARS	XADS	CDM
R	SNF7	SNF6	SNF5	SNF4	SNF3	SNF2	SNF1	SNF0
Reset	1	1	1	1	0	0	0	0

AVSEL [1:0]: ADC average times (for Carrier / temperature sensor / external ADC). Recommend AVSEL = [11].
[00]: No average.
[01]: Average 2 times.
[10]: Average 4 times.
[11]: Average 8 times.

MVSEL [1:0]: ADC average times (for VCO calibration and RSSI). Recommend MVSEL = [11].
[00]: Average 8 times.
[01]: Average 16 times.
[10]: Average 32 times.
[11]: Average 64 times.

RADC: ADC Read Out Average Mode.
[0]: 1, 2, 4, 8 average mode. The average number is according to the setting of AVSEL.
[1]: 8, 16, 32, 64 average mode. The average number is according to the setting of MVSEL.

FSARS: ADC Clock Select.
[0]: 4MHz.
[1]: 8MHz.

XADS: External ADC Input Signal Select.
[0]: Disable.
[1]: Enable.

CDM: RSSI measurement mode. Recommend CDM = [1].
[0]: Single mode.
[1]: Continuous mode.

SNF [7:0]: Sub-package Flag (read only).

9.2.33 Code Register I (Address: 20h) (AGT[3:0]=0, page 0)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--	WHTS	FECS	CRCS	IDL1	IDL0	EPML1	EPML0

R	SNF15	SNF14	SNF13	SNF12	SNF11	SNF10	SNF9	SNF8
Reset	0	0	0	0	0	1	1	1

WHTS: Data Whitening (Data Encryption) Select.
[0]: Disable.
[1]: Enable (The data is whitening by multiplying PN7).

FECS: FEC Select.
[0]: Disable.
[1]: Enable (The FEC is (7, 4) Hamming code).

CRCS: CRC Select.
[0]: Disable.
[1]: Enable. The CRC is set by CRCDNP (0x1A) for either CCITT-16 CRC or CRC-DNP

IDL [1:0]: ID Code Length Select. Recommend IDL= [11].
[00]: Reserved.
[01]: 4 bytes.
[10]: Reserved.
[11]: 8 bytes.
If user selects 4Bytes ID code, it is called SID1. If user selects 8Bytes ID code, the first 4Bytes ID code is called SID1 and the second 4Bytes ID code is called SID2.

EPML [1:0]: Extend Preamble Length Select. Recommend EPML= [00].
[00]: 0 byte.
[01]: 1 byte.
[10]: 2 bytes.
[11]: 4 bytes.

SNF [15:8]: Sub-package Flag (read only).

9.2.34 Code Register II (Address: 21h) (AGT[3:0]=0, page 0)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	MSCRC	EDRL	HECS	ETH2	ETH1	ETH0	PTH1	PTH0
R	MTCRCF7	MTCRCF6	MTCRCF5	MTCRCF4	MTCRCF3	MTCRCF2	MTCRCF1	MTCRCF0
Reset	0	0	0	0	0	1	1	0

MSCRC: Mask CRC (CRC Data Filtering Enable).
[0]: Disable.
[1]: Enable.

EDRL: Enable FIFO Dynamic Length
[0]: Disable.
[1]: Enable.

HECS: Head CRC Select
[0]: disable.
[1]: enable

ETH [2:0]: Received SID2 Code Error Tolerance. SID2 is only valid if ID length is 8bytes.
[000]: 0 bit,
[001]: 1 bit.
[010]: 2 bit.
[011]: 3 bit.
[100]: 4 bit,
[101]: 5 bit.
[110]: 6 bit.
[111]: 7 bit.

PTH [1:0]: Received SID1 Code Error Tolerance.
[00]: 0 bit,
[01]: 1 bit.
[10]: 2 bit.
[11]: 3 bit.

MTCRCF [7:0]: Sub-package CRC Flag (read only).

9.2.35 Code Register III (Address: 22h) (AGT[3:0]=0, page 0)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CRCINV	WS6	WS5	WS4	WS3	WS2	WS1	WS0
R	MTCRCF15	MTCRCF14	MTCRCF13	MTCRCF12	MTCRCF11	MTCRCF10	MTCRCF9	MTCRCF8
Reset	0	0	1	0	1	0	1	0

CRCINV: CRC Inverted Select.
[0]: Non-inverted.
[1]: inverted.

WS [6:0]: Data Whitening Seed (data encryption key).

MTCRCF [15:8]: Sub-package CRC Flag (read only).

9.2.36 IF Calibration Register I (Address: 23h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	HFR	CKGS1	CKGS0	MFBS	MFB3	MFB2	MFB1	MFB0
R	--	---	---	FBCF	FB3	FB2	FB1	FB0
Reset	1	1	1	0	0	1	1	0

HFR: Half frequency rate select.
[0]: 32x.
[1]: 16x.

CKGS [1:0]: Clock generator frequency (F_{MSYCK}) select. It should set F_{MSYCK}= 16*F_{IF}.
HFR=0:
[00]: 32MHz.
[01]: 64MHz.
[10]: 96MHz.
[11]: 128MHz.
HFR=1:
[00]: 16MHz.
[01]: 32MHz.
[10]: 48MHz.
[11]: 64MHz.

FBCF: IF Filter Band Auto Calibration Flag (read only).
[0]: Pass.
[1]: Fail.

FB [3:0]: IF filter bank (read only).

MFBS: IF Filter Calibration Select. Recommend MFBS = [0].
[0]: Auto calibration.
[1]: Manual Setting MFB [3:0].

MFB [3:0]: IF Filter Manual Calibration Value.

9.2.37 IF Calibration Register II (Address: 24h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PDNTXS	RAMPS2	RAMPS1	RAMPS0	DTDS3	DTDS2	DTDS1	DTDS0
R	--	--	--	FCD4	FCD3	FCD2	FCD1	FCD0
Reset	0	0	0	0	0	0	0	0

PDNTXS: TX Ramp down delay Select.
[0]: No delay
[1]: Delay 8us

RAMPS [2:0]: Reserved for internal usage only.

DTDS [3:0]: Direct mode TX data delay select.

Delay DTDS [3:0] master clocks.

FCD [4:0]: IF Filter Auto Calibration Deviation from Goal (read only).

9.2.38 VCO Current Calibration Register (Address: 25h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CSW	DEVCM	VCRLS	MVCS	VCOC3	VCOC2	VCOC1	VCOC0
R	--	--	--	VCCF	VCB3	VCB2	VCB1	VCB0
Reset	1	1	0	0	1	1	1	1

DEVCM: DEV calibration mode.
[0]: single side mode.
[1]: double side mode.

CSW: Clock Disable for VCO Modulation.
[0]: Enable.
[1]: Disable.

VCRLS: VCO Current Resistor Select.
[0]: low band.
[1]: high band.

MVCS: VCO current calibration value select.
[0]: Auto.
[1]: Manual.

VCOC [3:0]: VCO Current Bank Manual Calibration Value.
MVCS= 1: Manual VCO current bank.

VCCF: VCO Current Auto Calibration Flag (read only).
[0]: Pass.
[1]: Fail.

VCB [3:0]: VCO Current Bank Calibration Value (read only).
MVCS= 0: Auto calibration value (AVCB).
MVCS= 1: Manual calibration value (VCOC).

9.2.39 VCO Bank Calibration Register I (Address: 26h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	DCD1	DCD0	DAGS	MVBS	MVB3	MVB2	MVB1	MVB0
R	--	--	--	VBCF	VB3	VB2	VB1	VB0
Reset	1	1	0	0	1	0	0	0

DCD [1:0]: VCO Deviation Calibration Delay.
Delay time = PDL (Delay Register I, 17h) × (DCD + 1).

DAGS: DAG Calibration Value Select. Recommend DAGS = [0].
[0]: Auto calibration value.
[1]: Manual calibration value.

MVBS: Manual VCO Bank Select. Recommend MVBS = [0].
[0]: Auto calibration value (VB[2:0]).
[1]: Manual calibration value (MVB [2:0]).

MVB [3:0]: Manual VCO Band.
VCO frequency increases when MVB increases.

VBCF: VCO Band Auto Calibration Flag (read only).
[0]: Pass.
[1]: Fail.

VB [3:0]: VCO Bank Calibration Value (read only).
MVBS= 0: Auto calibration value (AVB).
MVBS= 1: Manual calibration value (MVB).

9.2.40 VCO Bank Calibration Register II (Address: 27h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	DAGM7	DAGM6	DAGM5	DAGM4	DAGM3	DAGM2	DAGM1	DAGM0
R	DAGB7	DAGB6	DAGB5	DAGB4	DAGB3	DAGB2	DAGB1	DAGB0
Reset	1	0	0	0	0	0	0	0

DAGM [7:0]: DAG Manual Setting Value. Recommend DAGM = [0x80].

DAGB [7:0]: Auto DAG Calibration Value (read only).

9.2.41 VCO Deviation Calibration Register I (Address: 28h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	DEVS3	DEVS2	DEVS1	DEVS0	DAMR_M	VMTE_M	VMS_M	MSEL
R	DEVA7	DEVA6	DEVA5	DEVA4	DEVA3	DEVA2	DEVA1	DEVA0
Reset	0	1	1	1	0	0	0	0

DEVA [7:0]: Deviation Output Value.
MVDS (29h)= 0: Auto calibration value ((DEVC / 8) × (DEVS + 1)),
MVDS (29h)= 1: Manual calibration value (DEVM [6:0]).

DEVS [3:0]: Deviation Output Scaling.

DAMR_M: DAMR Manual Enable. Recommend DAMR_M = [0].
[0]: Disable.
[1]: Enable.

VMTE_M: VMT Manual Enable. Recommend VMTE_M = [0].
[0]: Disable.
[1]: Enable.

VMS_M: VM Manual Enable. Recommend VMS_M = [0].
[0]: Disable.
[1]: Enable.

MSEL: VMS, VMTE and DAMR control select. Recommend MSEL = [0].
[0]: Auto control.
[1]: Manual control.

9.2.42 VCO Deviation Calibration Register II (Address: 29h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	MVDS	DEVM6	DEVM5	DEVM4	DEVM3	DEVM2	DEVM1	DEVM0
R	DEVC7	DEVC6	DEVC5	DEVC4	DEVC3	DEVC2	DEVC1	DEVC0
Reset	0	0	1	1	0	1	1	0

DEVC [7:0]: VCO Deviation Auto Calibration Value (read only).

MVDS: VCO Deviation Calibration Select. Recommend MVDS = [0].
[0]: Auto calibration value.
[1]: Manual calibration value.

DEVM [6:0]: VCO Deviation Manual Calibration Value.

9.2.43 DASP0 (Address: 2Ah)(AGT[3:0]=0, page 0)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	QLIM	PRS	--	--	--	--	--	FBOP
R								
Reset	0	0	--	--	--	--	--	0

QLIM: quick charge select for IF limiter amp.
[0]: enable.
[1]: disable.

PRS: Reserved for internal usage only.
FBOP: FBC finish clock reset select.

[0]: No reset.
[1]: Reset clock state after FBC finish.

9.2.44 DASP1 (Address: 2Ah) (AGT[3:0]=1, page 1)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RFBS	CKGU	IFTS	TRDC	LNAVR			INTPRC
R								
Reset	0	0	0	--	--			1

RFBS: RF Bank select.
[0]: Low bank
[1]: High bank

CKGU: High data rate clock select. Reserved for internal usage only.

IFTS: Reserved for internal usage only.

INTPRC: Internal PLL loop filter resistor and capacitor select. Recommend INTPRC = [1].
[0]: disable.
[1]: enable

9.2.45 DASP2 (Address: 2Ah) (AGT[3:0]=2, page 2)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	VTRB3	VTRB2	VTRB1	VTRB0	VMRB3	VMRB2	VMRB1	VMRB0
R								
Reset	0	0	0	0	0	0	0	0

VTRB [3:0]: Resistor Bank for VT RC Filtering.

VMRB [3:0]: Resistor Bank for VM RC Filtering.

9.2.46 DASP3 (Address: 2Ah) (AGT[3:0]=3, page 3)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0
R								
Reset	1	0	0	0	0	0	0	0

DCV [7:0]: Demodulator Fix mode DC value.

9.2.47 DASP4 (Address: 2Ah) (AGT[3:0]=4, page 4)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	VMG7	VMG6	VMG5	VMG4	VMG3	VMG2	VMG1	VMG0
R								
Reset	1	0	0	0	0	0	0	0

VMG [7:0]: VM Center Value for Deviation Calibration.

9.2.48 DASP5 (Address: 2Ah) (AGT[3:0]=5, page 5)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--	PKTH	PKT1	PKT0	PKS	PKIS1	PKIS0	IFPK
R								
Reset	--	0	0	0	1	0	0	0

PKTH: VCO Peak Detect Threshold.

PKT [1:0]: VCO Peak Detect Current Select.

PKS: VCO Current Calibration Mode Select.

PKIS [1:0]: AGC Peak Detect Current Select.

IFPK: AGC Amplifier Current Select.

9.2.49 DASP6 (Address: 2Ah) (AGT [3:0]=6, page 6)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--	HPLS			LOVRS	TXLO_HC	PAB_HCS	PA_HCS
R								
Reset	--	0			0	0	0	0

HPLS: High Power LNA Gain Select.
[0]: LGC= 3 in TX Mode.
[1]: LGC= 0 in TX Mode.

LOVRS: LO voltage reference select.

TXLO_HC: TX LO high current.

PAB_HCS: PA Buffer high current.

PA_HCS: PA high current.

9.2.50 DASP7 (Address: 2Ah) (AGT[3:0]=7, page 7)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	XDS	VRSEL	MS	MSCL4	MSCL3	MSCL2	MSCL1	MSCL0
R								
Reset	0	0	0	1	0	1	1	0

XDS: VCO Modulation Data Sampling Clock selection.
[0]: 8x over-sampling Clock**.**
[1]: XCPCK Clock.

VRSEL: RSSI compensation select.
[0]: No compensation.
[1]: Compensation by RX gain.

MS: AGC Manual scale select. Recommend MS = [0].
[0]: By (RL−RH).
[1]: By MSCL [4:0].

MSCL [4:0]: AGC Manual Scale setting.

9.2.51 DASP8 (Address: 2Ah) (AGT[3:0]=8, page 8)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	MRCT7	MRCT6	MRCT5	MRCT4	MRCT3	MRCT2	MRCT1	MRCT0
R	RCT7	RCT6	RCT5	RCT4	RCT3	RCT2	RCT1	RCT0
Reset	0	0	1	1	1	0	1	0

MRCT [7:0]: RO Bank manual calibration value (write only).
Manual setting when MRC =1.

RCT [7:0]: RO Bank auto calibration value (read only).

9.2.52 DASP9 (Address: 2Ah) (AGT[3:0]=9, page 9)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	TGNUM11	TGNUM10	TGNUM9	TGNUM8	MVS1	MVS0	MRCT9	MRCT8
R	NUMLH11	NUMLH10	NUMLH9	NUMLH8	--	--	RCT9	RCT8
Reset	1	0	0	0	1	1	1	0

MVS [1:0]: RO calibration moving average mode.
[00]: 1
[01]: 2
[10]: 4
[11]: 8

9.2.53 DASP10 (Address: 2Ah) (AGT[3:0]=10, page 10)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	TGNUM7	TGNUM6	TGNUM5	TGNUM4	TGNUM3	TGNUM2	TGNUM1	TGNUM0
R	NUMLH7	NUMLH6	NUMLH5	NUMLH4	NUMLH3	NUMLH2	NUMLH1	NUMLH0
Reset	0	0	0	0	0	0	0	0

NUMLH [11:0]: RO N Counter calibration result (read only).

TGNUM [11:0]: RO N Counter target (write only).
RO N Counter calibration goal or manual setting.

9.2.54 DASP11 (Address: 2Ah) (AGT[3:0]=11, page 11)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RCOT2	RCOT1	RCOT0	--	--	--	--	--
R								
Reset	1	0	0	--	--	--	--	--

RCOT[2:0]: Reserved for internal usage only.

9.2.55 DASP12(Address: 2Ah) (AGT[3:0]=12 page 12

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	MTCRCS	DRS	SPL1	SPL0	--	--	--	--
R								
Reset	0	0	0	0	--	--	--	--

MTCRCS: Multi-CRC select.
[0]: Disable.
[1]: Enable.

DRS: Data received select for MTCRC.
[0]: Package will be stored when CRC ok.
[1]: Package will be stored when package finish.

SPL: Sub-package length.
[00]: 32bytes.
[01]: 64bytes.
[10]: 128bytes.
[11]: 256bytes.

9.2.56 VCO Modulation Delay Register (Address: 2Bh)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	DMV1	DMV0	DEVFD2	DEVFD1	DEVFD0	DEVD2	DEVD1	DEVD0
R								
Reset	1	1	0	0	0	0	1	1

DMV [1:0]: Modulator D/A Voltage Range Select.
[00]: 1/32*1.2.
[01]: 1/16*1.2.
[10]: 1/8*1.2.
[11]: 1/4*1.2.

DEVFD [2:0]: VCO Modulation Data Delay by 8x over-sampling Clock.

DEVD [2:0]: VCO Modulation Data Delay by XCPCK Clock.

9.2.57 Battery Detect Register (Address: 2Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W		PM1S	BGS	QDS	BVT2	BVT1	BVT0	BD_E
R	--	--	--	BDF	BVT2	BVT1	BVT0	BD_E
Reset		0	0	1	0	0	1	0

PM1S: PM1 select.
[0]: Disable.
[1]: Enable.

BGS: Bangap (BG) select:
[0]: Low current BG.
[1]: High current BG.
Sleep mode should be set to [0].

BDF: Low Battery Detection Flag (read only).
[0]: battery low.
[1]: battery high.

QDS: VDD_A Quick Discharge Select. Recommend QDS = [1].
[0]: Disable.
[1]: Enable.

BVT [2:0]: Battery Voltage Threshold Select.
[000]: 2.0V,
[001]: 2.1V.
[010]: 2.2V.
[011]: 2.3V.
[100]: 2.4V.
[101]: 2.5V.
[110]: 2.6V.
[111]: 2.7V.

BD_E: Battery Detect Enable.
[0]: Disable.
[1]: Enable.

9.2.58 TX Test Register (Address: 2Dh)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	ASMV1	ASMV0	TXCS	--	--	TBF2	TBF1	TBF0
R								
Reset	1	1	1	--	--	1	1	1

ASMV [1:0]: Ramp up/down clock select.
[00]: 1 MHz.
[01]: 1/2 MHz.
[10]: 1/4 MHz.
[11]: 1/8 MHz.

TXCS: TX current setting.

TBF [2:0]: TX Buffer Setting.

Refer to A5133 App. Note for more settings.

9.2.59 RX DEM Test Register I (Address: 2Eh)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	DMT	DCM1	DCM0	CDPM	MXT	SLF2	SLF1	SLF0
R								
Reset	0	1	1	0	0	1	1	1

DMT: Reserved for internal usage only.

DCM [1:0]: Demodulator DC estimation mode. Recommend DCM = [10].
(The average length before hold is selected by DCL in **Code Register II**.)
[00]: DC set by DCV.
[01]: DC holds after SID1detected.
[10]: DC holds after FSYNC detected.
[11]: No hold.

CDPM: Reset time-out (40bits) counter after SID1 match.
[0]: Disable
[1]: Enable

MXT: Control the GPIO1 and CKO function (MXDEC, MXINC).
[0]: MXDEC=inverter signal of OKADC, MXINC = EOADC
[1]: MXDEC = DEC, MXINC = INC

SLF [2:0]: Reserved for internal usage only.

9.2.60 RX DEM Test Register II (Address: 2Fh)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	AGCH1	AGCH0	DCL2	DCL1	DCL0	RAW	--	MOVS
R								
Reset	1	1	1	1	0	0	--	0

AGCH [1:0]: AGC Hold mode. Recommend AGCH = [01].
[00]: by SID1 detect.
[01]: by frame sync (FSYNC) detect.
[10]: no hold.
[11]: by MAGC.

DCL2: DC Estimation Average Length After ID Detected. Recommend DCL2 = [1].
[0]: 128 bits.
[1]: 256 bits.

DCL [1:0]: DC Estimation Average Length Before ID Detected. Recommend DCL = [10].
[00]: 8 bits.
[01]: 16 bits.
[10]: 32 bits.
[11]: 64 bits.

RAW: Raw Data Output Select. Recommend RAW = [1].
[0]: latch data output.
[1]: RAW data output.

MOVS: Select the moving average data source from the last filter in demodulation.
[0]: Select date source from the output of the last filter.
[1]: Select date source from the input of the last filter.

9.2.61 Charge Pump Current Register I (Address: 30h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CPM3	CPM2	CPM1	CPM0	CPT3	CPT2	CPT1	CPT0
R								
Reset	1	1	1	1	0	0	1	1

CPM [3:0]: Charge Pump Current Setting for VM loop. Recommend CPM = [1111].
Charge pump current = (CPM + 1) / 16 mA.

CPT [3:0]: Charge Pump Current Setting for VT loop. Recommend CPT = [0011].
Charge pump current = (CPT + 1) / 16 mA.

9.2.62 Charge Pump Current Register II (Address: 31h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CPTX3	CPTX2	CPTX1	CPTX0	CPRX3	CPRX2	CPRX1	CPRX0
R								
Reset	0	0	1	1	0	0	1	1

CPTX [3:0]: Charge Pump Current Setting for TX mode. Recommend CPTX = [0011].
Charge pump current = (CPTX + 1) / 16 mA.

CPRX [3:0]: Charge Pump Current Setting for RX mode. Recommend CPRX = [0011].
Charge pump current = (CPRX + 1) / 16 mA.

9.2.63 Crystal Test Register (Address: 32h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--	CPS	CPCH1	CPCH0	CPCS	XCC	XCP1	XCP0
R								
Reset	--	1	0	0	1	1	0	1

CPS: PLL charge pump enable. Recommend CPS = [1].
[0]: Enable.
[1]: Disable.

CPCH [1:0]: Charge Pump High Current. Recommend CHCH = [00]

CPCS: Charge Pump Current Select. Recommend CPCS = [1].
[0]: Use CPM for TX, CPT for RX.
[1]: Use CPTX for TX, CPRX for RX.

XCC: Crystal Startup Current Selection. Recommend XCC = [1].
[0]: about 0.7 mA.
[1]: about 1.5 mA.

XCP [1:0]: Crystal Oscillator Regulated Couple Setting. Recommend XCP = [01].
[00]: 1.5mA.
[01]: 0.5mA.
[10]: 0.35mA.
[11]: 0.3mA.

9.2.64 PLL Test Register (Address: 33h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	MDEN	--	PRIC1	PRIC0	PRRC1	PRRC0	SDPW	NSDO
R								
Reset	0	--	0	1	0	1	0	1

MDEN : Use for Manual VCO Calibration.

PRIC [1:0]: Prescaler IF Part Current Setting.
[00]: 0.95mA.
[01]: 1.05mA.
[10]: 1.15mA.
[11]: 1.25mA.

PRRC [1:0]: Prescaler RF Part Current Setting.
[00]: 1.0mA.
[01]: 1.2mA.
[10]: 1.4mA.
[11]: 1.6mA.

SDPW : Clock Delay For Sigma Delta Modulator.
[0]: 13 ns.
[1]: 26 ns.

NSDO : Sigma Delta Order Setting.
[0]: order 2.
[1]: order 3.

9.2.65 VCO Test Register (Address: 34h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	DEVGD2	DEVGD1	DEVGD0	RLB1	RLB0	VBS2	VBS1	VBS0
R								
Reset	0	0	0	1	0	0	1	1

DEVGD [2:0]: Sigma Delta Modulator Data Delay Setting.

RLB [1:0]: RF divider Current Select.
[00]: 1.2mA.
[01]: 1.5mA.

[10]: 1.8mA.
[11]: 2.1mA.

VBS[2:0] : VCO Buffer Current Setting.
[000]: 0.5mA.
[001]: 1.0mA.
[010]: 1.5mA.
[011]: 2.0mA.
[100]: 2.5mA.
[101]: 3.0mA.
[110]: 3.5mA.
[111]: 4.0mA.

9.2.66 RF Analog Test Register (Address: 35h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	AGT3	AGT2	AGT1	AGT0	RFT3	RFT2	RFT1	RFT0
R								
Reset	0	0	0	0	0	0	0	0

AGT[3:0]: Page select.

RFT [3:0]: RF Analog Pin Configuration. Recommend RFT= [0000].

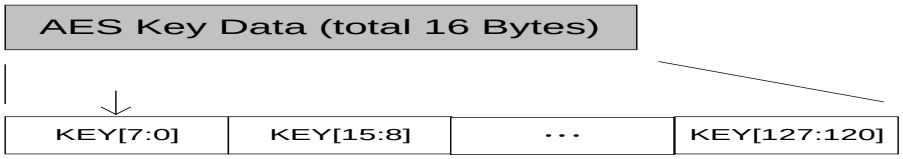
RFT[3:0]	VDD_R
[X000]	No connection
[X001]	No connection
[X010]	No connection
[X011]	RSSI voltage
[X100]	VDD_A voltage
[X101]	Analog temperature voltage
[0110]	IFTS=0, BPF positive I-phase output IFTS=1, IFA positive I-phase output
[0111]	IFTS=0, BPF negative I-phase output IFTS=1, IFA negative I-phase output
[1110]	IFTS=0, BPF positive I-phase output IFTS=1, Mixer positive I-phase output
[1111]	IFTS=0, BPF negative I-phase output IFTS=1, Mixer negative I-phase output

9.2.67 Key data Register (Address: 36h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	KEYI7	KEYI6	KEYI5	KEYI4	KEYI3	KEYI2	KEYI1	KEYI0
R	KEYO7	KEYO6	KEYO5	KEYO4	KEYO3	KEYO2	KEYO1	KEYO0
Reset	0	0	0	0	0	0	0	0

KEYI [7:0]: AES128 key input, total 16-btyes. (Write only).

KEYO [7:0]: AES128 key output, total 16-bytes. (Read only). Select by KEYOS (3Eh).



9.2.68 Channel Select Register (Address: 37h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CHI3	CHI2	CHI1	CHI0	CHD3	CHD2	CHD1	CHD0
R								
Reset	0	1	1	1	1	1	1	1

CHI [3:0]: Auto IF Offset Channel Number Setting.
$F_{CHSP} \times (CHI + 1) = F_{IF}$

CHD [3:0]: Channel Frequency Offset for Deviation Calibration.
Offset channel number = +/- (CHD + 1).

9.2.69 ROMP0 (Address: 38h)(AGT[3:0]=0, page 0)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	BDC5	BDC4	BDC3	BDC2	BDC1	BDC0	REGCL	PD_BOD
R								
Reset	0	0	0	0	0	0	0	0

BDC[5:0]: Battery detector current option select.

REGCL: Reserved for internal usage.

PD_BOD: BOD circuit power down.
[0]: Power on.
[1]: Power down.

9.2.70 ROMP1 (Address: 38h)(AGT[3:0]=1, page 1)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--	REGVS	--	FBG4	FBG3	FBG2	FBG1	FBG0
R	--	--	--	FBGR4	FBGR3	FBGR2	FBGR1	FBGR0
Reset	--	0	--	1	0	0	0	0

Reserved for internal usage.

9.2.71 ROMP2 (Address: 38h)(AGT[3:0]=2, page 2)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--	--	CTR5	CTR4	CTR3	CTR2	CTR1	CTR0
R	--	--	CTRR5	CTRR4	CTRR3	CTRR2	CTRR1	CTRR0
Reset	--	--	1	0	0	0	0	0

Reserved for internal usage.

9.2.72 ROMP3 (Address: 38h)(AGT[3:0]=3, page 3)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	FGC1	FGC0	SRS2	SRS1	SRS0	CRS2	CRS1	CRS0
R	--	--	SRSR2	SRSR1	SRSR0	CRSR2	CRSR1	CRSR0
Reset	1	1	1	0	0	1	0	0

Reserved for internal usage.

9.2.73 ROMP4 (Address: 38h)(AGT[3:0]=4, page 4)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--	STMP	STM5	STM4	STM3	STM2	STM1	STM0
R	--	STMP	STMR5	STMR5	STMR3	STMR2	STMR1	STMR0
Reset	--	0	1	0	0	0	0	0

Reserved for internal usage.

9.2.74 ROMP5 (Address: 38h)(AGT[3:0]=5, page 5)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CDPS	CDPN	PMPN	--	DEVSUB	FPS2	FPS1	FPS0
R								
Reset	0	1	0	--	0	0	0	0

CDPS: TX carrier replace by preamble (0101).
[0]: Disable.
[1]: Enable.

CDPN: TX carrier replace by PN code.
[0]: Disable.
[1]: Enable.

PMPN: Preamble replace by PN code.
[0]: Disable.
[1]: Enable.

DEVSUB: TX deviation scale.
[0]: 1x.
[1]: 0.9x.

FPS[2:0]: GF parameter select.
GDR=0

FPS[2:0]	7	6	5	4	3	2	1	0
BT	0.7	0.65	0.6	0.55	0.375	0.35	0.325	0.3

9.2.75 ROMP6 (Address: 38h)(AGT[3:0]=6, page 6)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	TGM7	TGM6	TGM5	TGM4	TGM3	TGM2	TGM1	TGM0
R								
Reset	0	1	1	0	1	1	1	0

TGM [7:0]: VCO bank VT margin.

9.2.76 ROMP7 (Address: 38h)(AGT[3:0]=7, page 7)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	DVO15	DVO14	DVO13	DVO12	DVO11	DVO10	DVO9	DVO8
R								
Reset	0	0	0	0	1	0	0	0

9.2.77 ROMP8 (Address: 38h)(AGT[3:0]=8, page 8)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	DVO7	DVO6	DVO5	DVO4	DVO3	DVO2	DVO1	DVO0
R								
Reset	0	0	0	0	0	0	0	0

DVO [15:0]: PLL channel step setting.

9.2.78 ROMP9 (Address: 38h)(AGT[3:0]=9, page 9)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	EFSW	EFWE	EFRE	--	--	EFB2	EFB1	EFB0
R								
Reset	0	0	0	--	--	0	0	0

EFSW: Efuse function switch. (For address 0x3F).
[0]: USID.
[1]: Efuse.

EFWE: Efuse Write enable. (For address 0x3F). (Auto clear when done).
[0]: Disable.
[1]: Enable.

EFRE: Efuse Read enable. (For address 0x3F).
[0]: Disable.
[1]: Enable.

EFB[2:0]: Efuse Write data point. (For address 0x3F).

9.2.79 ROMP10 (Address: 38h)(AGT[3:0]=10, page 10)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--	PSDS2	PSDS1	PSDS0	PDNFH	QDSFH	PDNFL	QDSFL
R								
Reset	--	0	1	1	1	0	1	0

PSDS[2:0]: Power saving signal delay select for VDD_P.

QDFSH, PDNFH, QDSFL, PDNFL: Efuse power control.

9.2.80 ROMP11 (Address: 38h)(AGT[3:0]=11, page 11)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--	--	--	--	--	--	CBIST	BIST
R	BER7	BER6	BER5	BER4	BER3	BER2	BER1	BER0
Reset	--	--	--	--	--	--	0	0

CBIST: TX continuous PN9 output.
[0]: Disable.
[1]: Enable.

BIST: RX PN9 BER test.
[0]: Disable.
[1]: Enable.
BER[7:0]:RX bit error rate output.

9.2.81 Data Rate Clock Register (Address: 39h)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
R								
Reset	0	0	0	0	0	0	0	0

SDR [7:0]: Data Rate Setting. On-air Data rate = FIF / (SDR+1).

9.2.82 FCR Register (Address: 3Ah)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	FCL1	FCL0	ARC3	ARC2	ARC1	ARC0	EAK	EAR
R	ARTEF	VPOAK	RCR3	RCR2	RCR1	RCR0	EAK	EAR
Reset	0	0	0	1	1	0	0	0

FCL [1:0]: Frame Control Length.
[00]: No Frame Control
[01]: 1 byte Frame Control. (FCB0)
[10]: 2 byte Frame control. (FCB0+FCB1)
[11]: 4 byte Frame control. (FCB0+FCB1+FCB2+FCB3)

RCR [3:0]: Decremented ARC[3:0] (read only).

ARC [3:0] : Auto Resend Cycle Setting.
[0000]: resend disable.
[0001]: 1
[0010]: 2
[0011]: 3

[0100]: 4
[0101]: 5
[0110]: 6
[0111]: 7
[1000]: 8
[1001]: 9
[1010]: 10
[1011]: 11
[1100]: 12
[1101]: 13
[1110]: 14
[1111]: 15

EAK: Enable auto-ack.
[0]: Disable.
[1]: Enable.

EAR: Enable auto-resend.
[0]: Disable.
[1]: Enable.

ARTEF: Auto re-transmission ending flag (read only).
[0]: Resend not end
[1]: Finish resend.

VPOAK: Valid Packet or ACK OK Flag. (read only)
This bit is clear by any Strobe command.
[0]: Neither valid packet nor ACK OK.
[1]: Valid packet or ACK OK.

9.2.83 ARD Register (Address: 3Bh)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	ARD7	ARD6	ARD5	ARD4	ARD3	ARD2	ARD1	ARD0
R								
Reset	0	0	0	0	0	0	1	1

ARD [7:0] : Auto Resend Delay
ARD Delay = 200 us * (ARD+1) □ (200us ~ 51.2 ms)

[0000-0000]: 200 us.
[0000-0001]: 400 us.
[0000-0010]: 600 us.
…
[1111-1111]: 51.2 ms.

9.2.84 AFEP Register (Address: 3Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	EAF	SPSS	ACKFEP5	ACKFEP4	ACKFEP3	ACKFEP2	ACKFEP1	ACKFEP0
R	-	-	EARTS2	EARTS1	EARTS0	TXSN2	TXSN1	TXSN0
Reset	1	1	0	0	0	0	1	1

EAF: Enable ACK FIFO.
[0]: Disable.
[1]: Enable.

SPSS: Mode Back Select when auto-act and auto-resend are enabled.
[0]: Reserved.
[1]: PLL mode.

ACKFEP [5:0]: FIFO Length setting for auto-ack packet.
ACK FIFO Length = (ACKFEP [5:0] + 1)
max. 64 bytes.

EARTS [2:0]: Enable Auto Resend Read.

TXSN [2:0]: TX Serial Number.
This device increases TXSN each time for every new packet and keep the same TXSN when retransmitting.

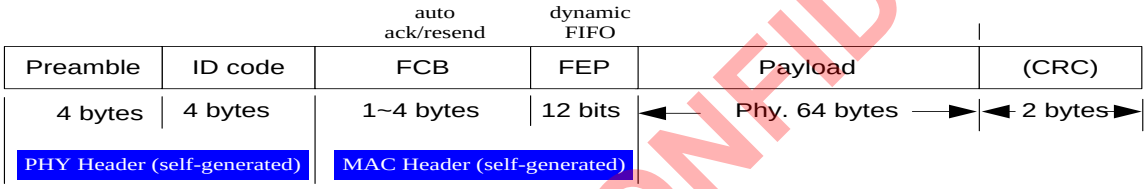
9.2.85 FCB Register (Address: 3Dh)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	FCB7	FCB6	FCB5	FCB4	FCB3	FCB2	FCB1	FCB0
R	FCB7	FCB6	FCB5	FCB4	FCB3	FCB2	FCB1	FCB0
Reset	0	0	0	0	0	0	0	0

FCB [7:0]: Frame Control Buffer, total 20-bytes.

Byte	Name	Bit-Map								Description	Strobe Cmd
0	FCB0	0	0	1	1	1	TXSN2	TXSN1	TXSN0	For auto-resend.	NA
1	FCB1	[7:0]								ACK info by user's attaching	NA
2	FCB2	[7:0]									
3	FCB3	[7:0]									

Remark:
1. TXSN is auto incremental for every new packet if FCB0 is enabled.
2. FCB0 ~ FCB3 is controlled by FCL[1:0] (3Ah)
3. User can attach wanted ACK information to FCB1 ~ FCB3 if auto-ack is enabled (EAK =1).



9.2.86 KEYC Register (Address: 3Eh)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	KEYOS	AFIDS	ARTMS	MIDS	AESS	--	AKFS	EDCRS
R								
Reset	0	0	0	0	0	0	0	0

KEYOS: AES128 Key source read select.
[0]: If AKFS=1, from RX received encrypted AES128 key data; If AKFS=0, from SPI write AES128 key data.
[1]: From encrypted/decrypted AES128 key data.

AFIDS: FIFO ID appendixes select.
[0]: Disable.
[1]: Enable.

ARTMS: auto-resend duration select.
[0]: random interval.
[1]: fixed interval.

MIDS: FIFO control byte address mapping for FIFO ID select.
[0]: Received device ID.
[1]: internal FIFO control byte ID.

AESS: encryption format selection.
[1]: Standard AES 128 bit.
[0]: proprietary 32 bit.

AKFS: Data packet with decrypted key appendixes select.
[0]: Disable.
[1]: Enable.

EDRCS: Data encrypt or decrypt select.
[0]: Disable.
[1]: Enable.

9.2.87 USID Register (Address: 3Fh)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	RND7	RND6	RND5	RND4	RND3	RND2	RND1	RND0
R	USID	USID	USID	USID	USID	USID	USID	USID
Reset								

RND [7:0]: Random seed for auto-resend interval.

USID [31:0]: USID= A1513300.

9.2.88 DSSS4 Register (Address: 20h)(AGT[3:0]=4, page 4)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								DSSS
R								
Reset								0

DSSS: Reserved. It should be set to 0.

9.2.89 EXT1 Register (Address: 21h)(AGT[3:0]=6, page 6)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PDNPAS	VRPL[2]	VRPL[1]	VRPL[0]	VBPAS_BF	VBPAS	TXLB[1]	TXLB[0]
R								
Reset	1	0	0	0	0	0	0	0

PDNPAS: PA regulator select.
[0]: Deselect.
[1]: Select.

VRPL [2:0]: internal PLL loop filter resistor value select.
[000]: 860 ohm.
[001]: 1.3K ohm.
[010]: 2K ohm.
[011]: 3K ohm.
[100]: 4.4K ohm.
[101]: 6.25K ohm.
[110]: 9.75K ohm.
[111]: 14.2K ohm.

VBPAS_BF, VBPAS: Reserved for internal usage only.

TXLB [1:0]: RF TX LO Buffer Current Select.

9.2.90 EXT2 Register (Address: 21h)(AGT[3:0]=8, page 8)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--	TPA[2]	TPA[1]	TPA[0]	SWM	RFINE[2]	RFINE[1]	RFINE[0]
R								
Reset	--	0	0	0	0	0	0	0

TPA [2:0]: PA Current Setting.

SWM: Selection of 32kHz oscillator. (Reserved for internal usage)

RFINE[2:0]: RC-OSC fine tuned value.

9.2.91 EXT3 Register (Address: 21h)(AGT[3:0]=9, page 9)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PORIPS	PMPAR	PM1SWE	PM1SW[1]	PM1SW[0]	PGV_PA[2]	PGV_PA[1]	PGV_PA[0]
R								
Reset	0	0	0	0	0	1	0	0

PORIPS: Reserved for internal usage.

PMPAR: PM1 switch gating.
[0]: All switch on.
[1]: Switch control by PM1SWE.

PM1SW[1:0]: PM1 switch select.
[00]: IF SW ON.
[01]: PLL SW ON.
[10]: RX SW ON.
[11]: TX SW ON.

PM1SWE: PM1 switch enable.
[0]: Disable.
[1]: Enable.

PGV_PA[2:0]: Power gain voltage for PA.
[000]: 1.2V.
[001]: 1.4V.
[010]: 1.6V.
[011]: 1.8V.
[100]: 2.0V.
[101]: 2.2V.
[110]: 2.4V.
[111]: 2.5V.

9.2.92 EXT4 Register (Address: 21h)(AGT[3:0]=10, page 10)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	IGM[3]	IGM[2]	IGM[1]	IGM[0]	ICONTROL[1]	ICONTROL[0]	IBPAS	ENRC
R								
Reset	0	0	0	0	0	0	0	0

IGM[3:0]: Adjusts current of the comparator in IRC. (Reserved for internal usage)

ICONTROL[1:0]: Reserved for internal usage only.

IBPAS: Reserved for internal usage only.

ENRC: Enable Internal XRC oscillator.
[0]: Disable.
[1]: Enable.

9.2.93 EXT5 Register (Address: 21h)(AGT[3:0]=11, page 11)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	KICS[1]	KICS[0]	CPM[1]	CPM[0]	CI[1]	CI[0]	CBBF[1]	CBBF[0]
R								
Reset	0	0	0	0	0	0	0	0

KICS[1:0]: Enable kick-off circuit select.
[00]:0us;
[01]:10us;
[1x]:20us.

CPM[1:0]: Reduces frequency of IRC for 8 second application. (Reserved for internal usage)

CI[1:0]: Reserved for internal usage only.

CBBF[1:0]: Reserved for internal usage only.

9.2.94 EXT6 Register (Address: 21h)(AGT[3:0]=12, page 12)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CSXTL[7]	CSXTL[6]	CSXTL[5]	CSXTL[4]	CSXTL[3]	CSXTL[2]	CSXTL[1]	CSXTL[0]
R								

Reset	0	1	1	0	0	1	0	0

CSXTL[7:0]: On-chip capacitor added on XI, XO pin, respectively.
CSXTL is the on-chip capacitor for XTAL oscillator to fine tune offset frequency of the wanted RF carrier.

9.2.95 EXT7 Register (Address: 22h)(AGT[3:0]=1, page 1)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	TXHP	BGCS	BIAS	TXLPN	PSDPAS[2]	PSDPAS[1]	PSDPAS[0]	XRCS
R								
Reset	0	0	0	0	1	1	1	0

TXHP: TX high power select.
[0]: Deselect.
[1]: Select.

BGCS: BG OP current select. Reserved for internal usage.

BIAS: Reserved for internal usage.

TXLPN: TX low power select.
[0]: Select.
[1]: Deselect.

PSDPAS[2:0]: power saving signal delay select for VDD_PA.

XRCS: Reserved for internal usage.

9.2.96 EXT8 Register (Address: 22h) (AGT[3:0]=2, page 2)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	MTRIM7	MTRIM6	MTRIM5	MTRIM4	MTRIM3	MTRIM2	MTRIM1	MTRIM0
R	TRIM7	TRIM6	TRIM5	TRIM4	TRIM3	TRIM2	TRIM1	TRIM0
Reset	0	0	0	0	0	0	0	0

MTRIM [8:0]: XRC Bank manual calibration value (write only).
Manual setting when MXRC =1.

TRIM [8:0]: XRC Bank auto calibration value (read only).

9.2.97 EXT9 Register (Address: 22h) (AGT[3:0]=3, page 3)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	PGV_P1	PGV_P0	EKIC_SEL1	EKICS_SEL 0				MTRIM8
R								TRIM8
Reset	0	0	0	0				1

EKIC_SEL [1:0]: Kick-off time.
[00]: 0us
[01]: 10us
[1x]: 20us

PGV_P[1:0]: VDD_P voltage select.
[00]: 1.2V.
[01]: 1.25V.
[10]: 1.3V.
[11]: 1.35V.

9.2.98 EXT10 Register (Address: 22h) (AGT[3:0]=4, page 4)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	TGNUM1_7	TGNUM1_6	TGNUM1_5	TGNUM1_4	TGNUM1_3	TGNUM1_2	TGNUM1_1	TGNUM1_0

R	NUMLH1_7	NUMLH1_6	NUMLH1_5	NUMLH1_4	NUMLH1_3	NUMLH1_2	NUMLH1_1	NUMLH1_0
Reset	0	0	0	0	0	0	0	0

NUMLH1 [1:0]: XRC N Counter calibration result (read only).

TGNUM1 [10:0]: XRC N Counter target (write only).
XRC N Counter calibration goal or manual setting.

9.2.99 EXT11 Register (Address: 22h) (AGT[3:0]=5, page 5)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W		REGCL_PA	MVS1_1	MVS1_0	MXRC	TGNUM1_10	TGNUM1_9	TGNUM1_8
R					--	NUMLH1_10	NUMLH1_9	NUMLH1_8
Reset		0	0	0	0	0	0	0

REGCL_PA: Reserved for internal usage.

MVS1 [1:0]: XRC calibration moving average mode.
[00]: 1
[01]: 2
[10]: 4
[11]: 8

MXRC: Manual XRC Bank value setting.
[0]: Auto.
[1]: Manual.

10. SPI

A5133 only supports one SPI interface with maximum data rate up to 10Mbps. MCU should assert SCS pin low (SPI chip select) to active accessing of A5133. Via SPI interface, user can access **control registers** and issue **Strobe command**. Figure 10.1 gives an overview of SPI access manners.

3-wire SPI (SCS, SCK and SDIO) or 4-wire SPI (SCS, SCK, SDIO and GIO1/GIO2) configuration is provided. For 3-wire SPI, SDIO pin is configured as bi-direction to be data input and output. For 4-wire SPI, SDIO pin is data input and GIO1 (or GIO2) pin is data output. In such case, GIO1S (0bh) or GIO2S (0ch) should be set to [0110].

For SPI write operation, SDIO pin is latched into A5133 at the rising edge of SCK. For SPI read operation, if input address is latched by A5133, data output is aligned at falling edge of SCK. Therefore, MCU can latch data output at the rising edge of SCK.

To control A5133's internal state machine, it is very easy to send Strobe command via SPI interface. The Strobe command is a unique command set with total 8 commands. See section 10.3, 10.4 and 10.5 for details.

	SPI chip select	Data In	Data Out
3-Wire SPI	SCS pin = 0	SDIO pin	SDIO pin
4-Wire SPI	SCS pin = 0	SDIO pin	GIO1 (GIO1S=0110) / GIO2 (GIO2S=0110)

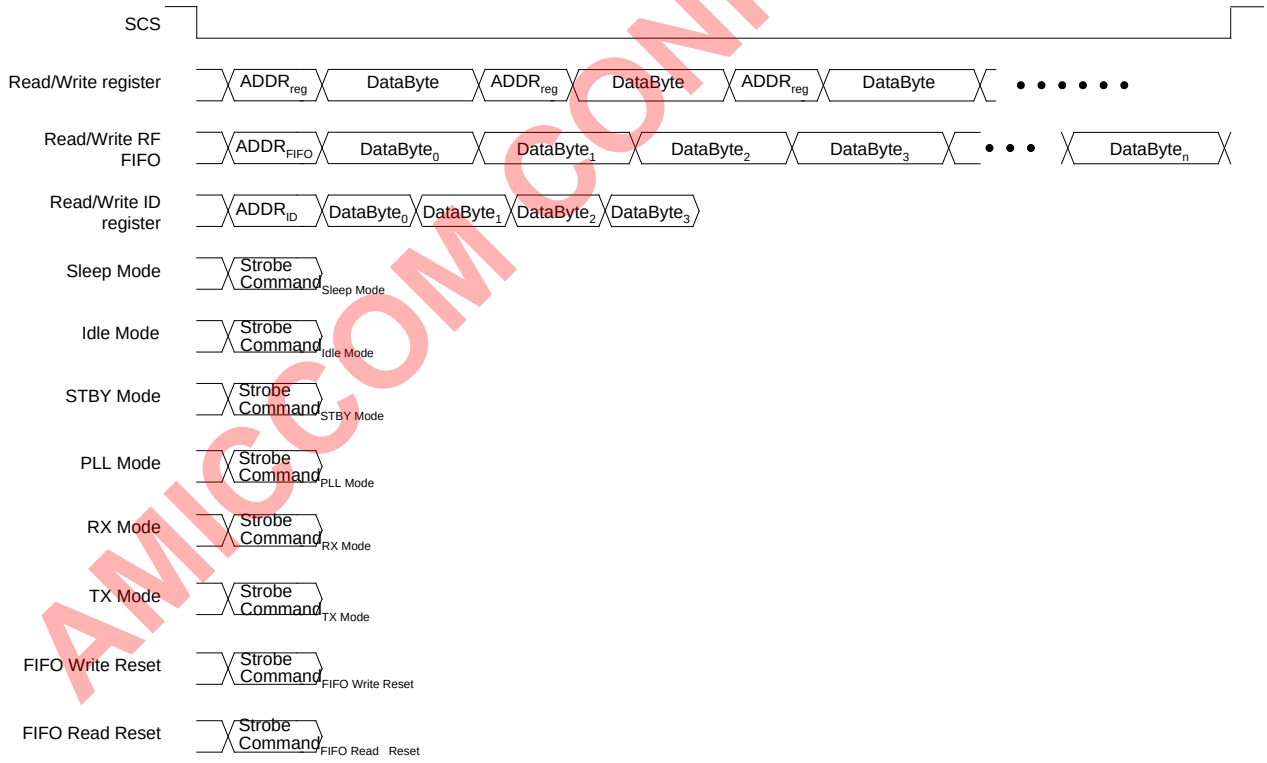


Figure 10.1 SPI Access Manners

10.1 SPI Format

The first bit (A7) is critical to indicate A5133 the following instruction is “Strobe command” or “control register”. See Table 10.1 for SPI format. Based on Table 10.1, To access control registers, just set A7=0, then A6 bit is used to indicate read (A6=1) or write operation (A6=0). See Figure 10.2 (3-wire SPI) and Figure 10.3 (4-wire SPI) for details.

Address Byte (8 bits)								Data Byte (8 bits)							
CMD	R/W	Address						Data							
A7	A6	A5	A4	A3	A2	A1	A0	7	6	5	4	3	2	1	0

Table 10.1 SPI Format

Address byte:

Bit 7: Command bit
[0]: Control registers.
[1]: Strobe command.

Bit 6: R/W bit
[0]: Write data to control register.
[1]: Read data from control register.

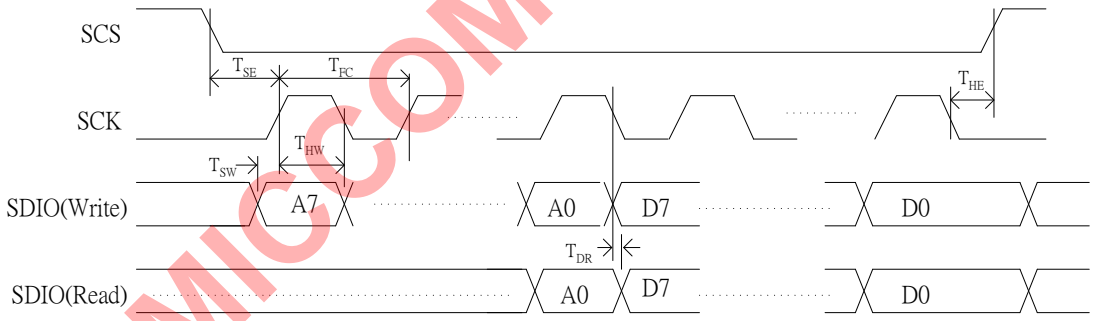
Bit [5:0]: Address of control register

Data Byte:

Bit [7:0]: SPI input or output data, see Figure 10.2 and Figure 10.3 for details.

10.2 SPI Timing Characteristic

No matter 3-wire or 4-wire SPI interface is configured, the maximum SPI data rate is 10 Mbps. To active SPI interface, SCS pin must be set to low. For correct data latching, user has to take care hold time and setup time between SCK and SDIO. See Table 10.2 for SPI timing characteristic.



Parameter	Description	Min.	Max.	Unit
T_{FC}	Frequency clock [*1].		10	MHz
T_{SE}	Enable setup time.	50		ns
T_{HE}	Enable hold time.	50		ns
T_{SW}	TX Data setup time.	50		ns
T_{HW}	TX Data hold time.	50		ns
T_{DR}	RX Data delay time.	0	50	ns

Table 10.2 SPI Timing Characteristic

Note 1: SPI frequency clock should be slower than BBCLK(0Ch).

10.3 SPI Timing Chart

In this section, 3-wire and 4-wire SPI interface read / write timing are described.

10.3.1 Timing Chart of 3-wire SPI

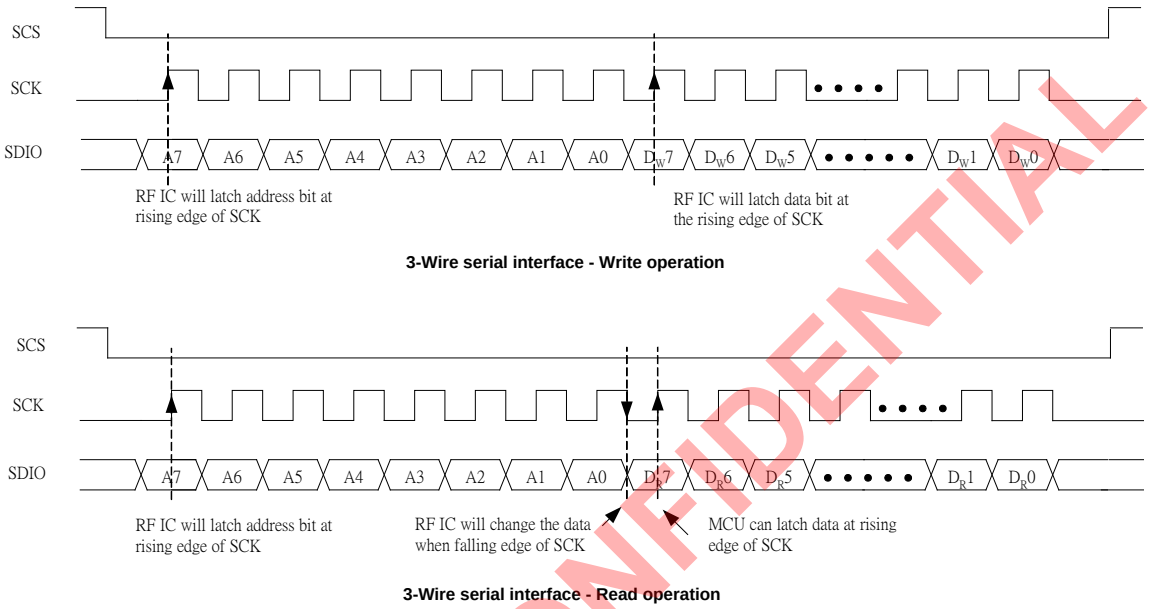


Figure 10.2 Read/Write Timing Chart of 3-Wire SPI

10.3.2 Timing Chart of 4-wire SPI

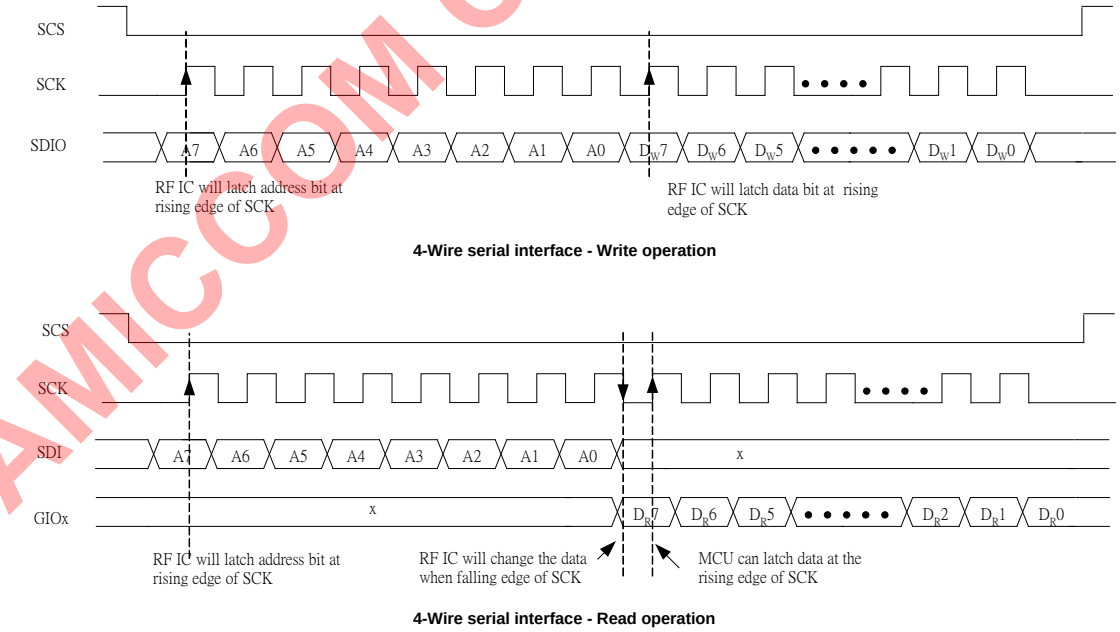


Figure 10.3 Read/Write Timing Chart of 4-Wire SPI

10.4 Strobe Commands

A5133 supports 8 Strobe commands to control internal state machine for chip's operations. Table 10.3 is the summary of Strobe commands.

Be notice, Strobe command could be defined by 8-bits (A7~A0). If 8-bits Strobe command is selected, A3 ~ A0 are don't care conditions. In such case, SCS pin can be remaining low for asserting next commands.

Strobe Command when AFIDS =0 (3Eh) and MIDS =0 (3Eh)

Strobe Command								**Description**
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	x	x	x	x	Sleep mode
1	0	0	1	x	x	x	x	Idle mode
1	0	1	0	x	x	x	x	Standby mode
1	0	1	1	x	x	x	x	PLL mode
1	1	0	0	x	x	x	x	RX mode
1	1	0	1	x	x	x	x	TX mode
1	1	1	0	x	x	x	x	FIFO write pointer reset
1	1	1	1	x	x	x	x	FIFO read pointer reset

Remark: x means " don't care"

Table 10.3 Strobe Commands by SPI interface

10.4.1 Strobe Command - Sleep Mode

Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								**Description**
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	x	x	x	x	Sleep mode

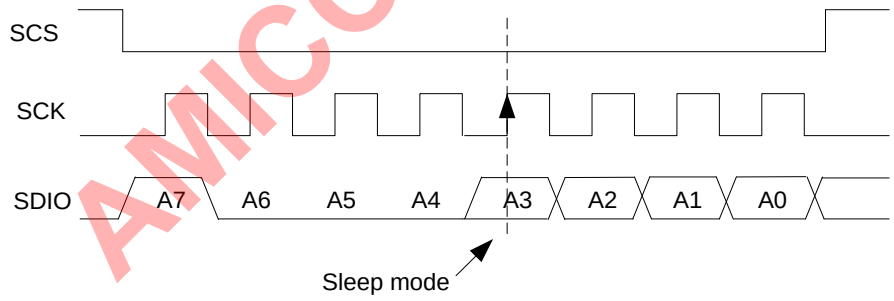


Figure 10.4 Sleep mode Command Timing Chart

10.4.2 Strobe Command - Idle Mode

Below is the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	1	x	x	x	x	Idle mode

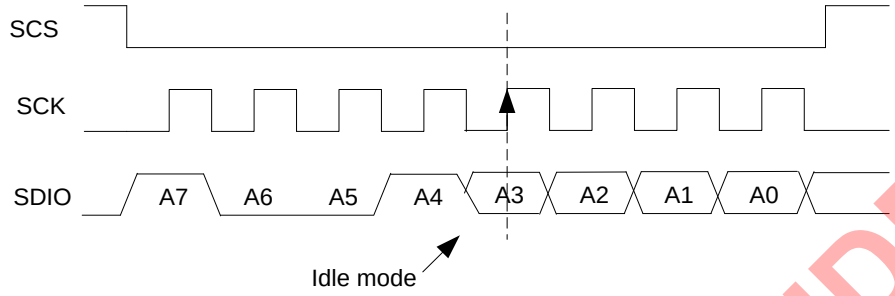


Figure 10.5 Idle mode Command Timing Chart

10.4.3 Strobe Command - Standby Mode

Below is the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	1	0	x	x	x	x	Standby mode

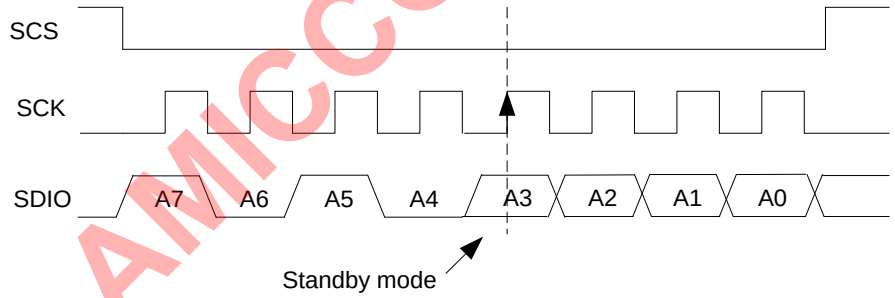


Figure 10.6 Standby mode Command Timing Chart

10.4.4 Strobe Command - PLL Mode

Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	1	1	x	x	x	x	PLL mode

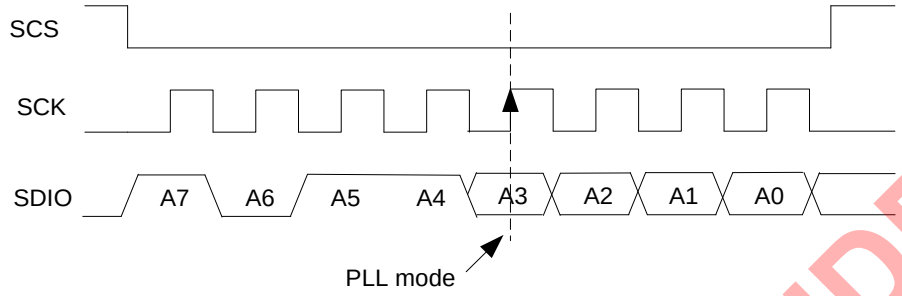


Figure 10.7 PLL mode Command Timing Chart

10.4.5 Strobe Command - RX Mode

Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	0	x	x	x	x	RX mode

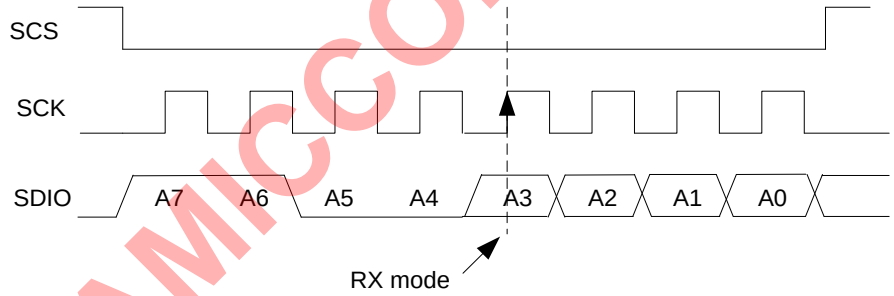


Figure 10.8 RX mode Command Timing Chart

10.4.6 Strobe Command - TX Mode

Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	1	x	x	x	x	TX mode

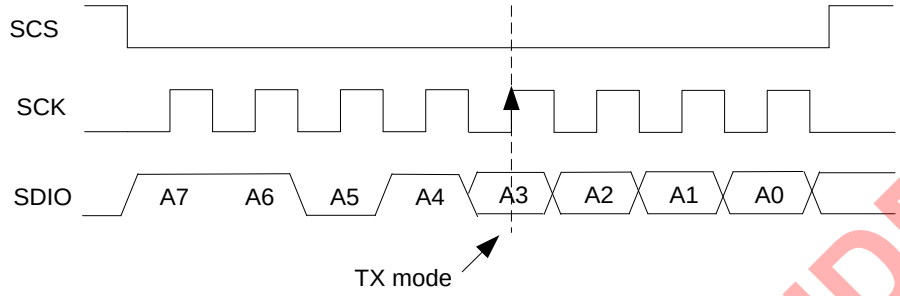


Figure 10.9 TX mode Command Timing Chart

10.4.7 Strobe Command – FIFO Write Pointer Reset

Below is the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	1	0	x	x	x	x	FIFO write pointer reset

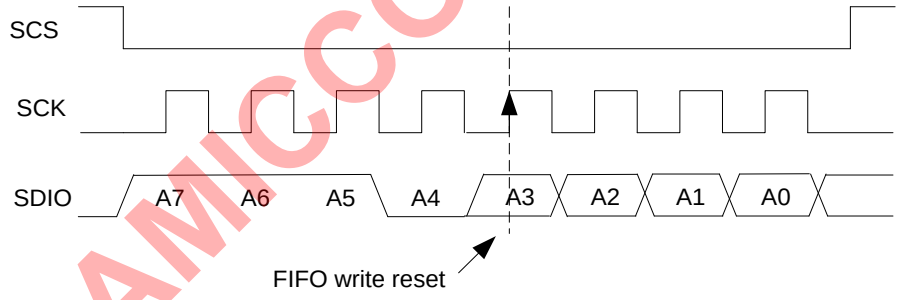


Figure 10.10 FIFO write pointer reset Command Timing Chart

10.4.8 Strobe Command – FIFO Read Pointer Reset

Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	1	1	x	x	x	x	FIFO read pointer reset

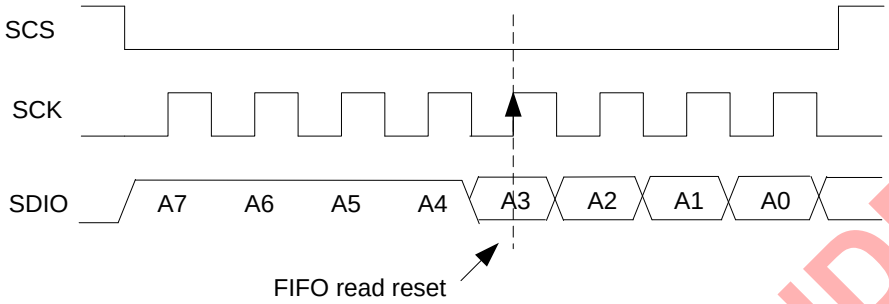


Figure 10.11 FIFO read pointer reset Command Timing Chart

10.5 Reset Command

In addition to power on reset (POR), MCU could issue software reset to A5133 by setting Mode Register (00h) through SPI interface as shown below. As long as 8-bits address (A7~A0) are delivered zero and data (D7~D0) are delivered zero, A5133 is informed to generate internal signal “RESETN” to initial itself. After reset command, A5133 is in standby mode and calibration procedure shall be issued again.

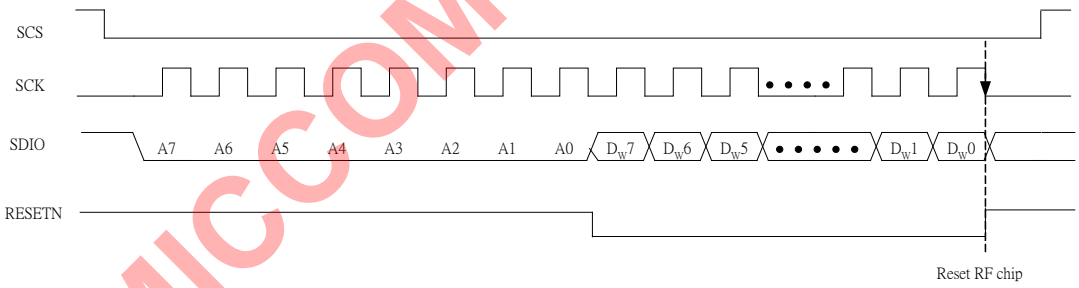


Figure 10.14 Reset Command Timing Chart

10.6 ID Accessing Command

A5133 has built-in 64-bits ID Registers for customized identification code. It is accessed via SPI interface. ID length is recommended to be 64 bits by setting IDL (1Fh). Therefore, user can toggle SCS pin to high to terminate ID accessing command when ID data is output completely.

Figure 10.15 and 10.16 are timing charts of 64-bits ID accessing via 3-wire SPI.

10.6.1 ID Write Command

User can refer to Figure 10.2 for SPI write timing chart in details. Below is the procedure of ID write command.

Step1: Deliver A7~A0 = 00000110 (A6=0 for write, A5~A0 = 000110 for ID addr, 06h).
Step2: By SDIO pin, deliver 64-bits ID into A5133 in sequence by Data Byte 0, 1, 2,3,4,5,6 and 7.

Step3: Toggle SCS pin to high when step2 is completed.

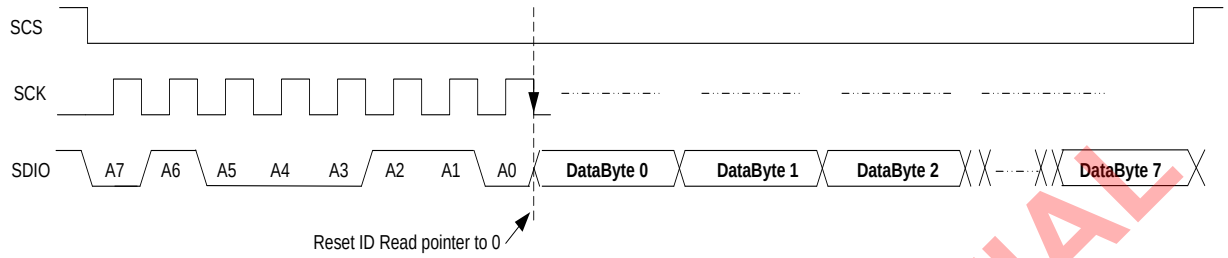


Figure 10.15 ID Write Command Timing Chart

10.6.2 ID Read Command

User can refer to Figure 10.2 for SPI read timing chart in details. Below is the procedure of ID read command.

Step1: Deliver A7~A0 = 01000110 (A6=1 for read, A5~A0 = 000110 for ID addr, 06h).
Step2: SDIO pin outputs 64-bits ID in sequence by Data Byte 0, 1, 2, 3, 4, 5, 6 and 7.
Step3: Toggle SCS pin to high when step2 is completed.

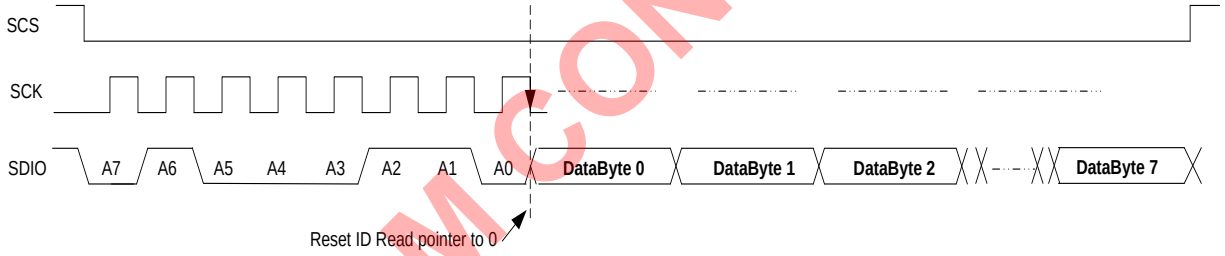


Figure 10.16 ID Read Command Timing Chart

10.7 FIFO Accessing Command

To use A5133's FIFO mode, enable FMS (01h) =1 via SPI interface. Before TX delivery, just write wanted data into TX FIFO (05h) then issue TX Strobe command. Similarly, user can read RX FIFO (05h) once payload data is received.

MCU can use polling or interrupt scheme to do FIFO accessing. FIFO status can output to GIO1 (or GIO2) pin by setting GIO1S (0Bh) or GIO2S (0Ch).

Figure 10.15 and 10.16 are timing charts of FIFO accessing via 3-wire SPI.

10.7.1 TX FIFO Write Command

User can refer to Figure 10.2 for SPI write timing chart in details. Below is the procedure of TX FIFO write command.

Step1: Deliver A7~A0 = 00000101 (A6=0 for write control register and issue FIFO A [5:0] = 05h).
Step2: By SDIO pin, deliver (n+1) bytes TX data into TX FIFO in sequence by Data Byte 0, 1, 2 to n.
Step3: Toggle SCS pin to high when step2 is completed.
Step4: Send Strobe command of TX mode (Figure 10.9) to do TX delivery.

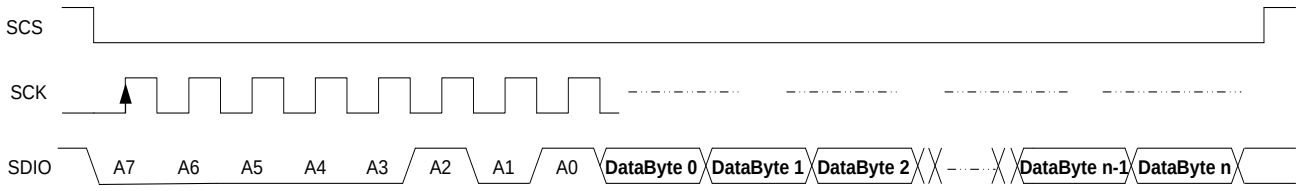


Figure 10.17 TX FIFO Write Command Timing Chart

10.7.2 Rx FIFO Read Command

User can refer to Figure 10.2 for SPI read timing chart in details. Below is the procedure of RX FIFO read command.

Step1: Deliver A7~A0 = 01000101 (A6=1 for read control register and issue FIFO at address 05h).
Step2: SDIO pin outputs RX data from RX FIFO in sequence by Data Byte 0, 1, 2 to n.
Step3: Toggle SCS pin to high when RX FIFO is read completely.

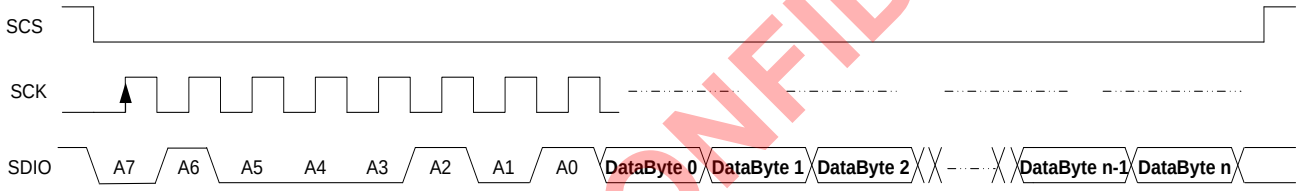


Figure 10.18 RX FIFO Read Command Timing Chart

11. State machine

From accessing data point of view, if FMS=1, FIFO mode is enabled, otherwise, A5133 is in direct mode.

	SPI chip select	SPI Clock	SPI Data In	SPI Data Out	FMS register
3-Wire SPI	SCS	SCK	SDIO	SDIO	FIFO (FMS=1) Direct (FMS=0)
4-Wire SPI	SCS	SCK	SDIO	GIO1 or GIO2	FIFO (FMS=1) Direct (FMS=0)

From current consumption point of view, A5133 has below 7 operation modes.

(1) Sleep mode
(2) Idle mode
(3) Standby mode
(4) PLL mode
(5) TX mode
(6) RX mode
(7) Star-networking mode

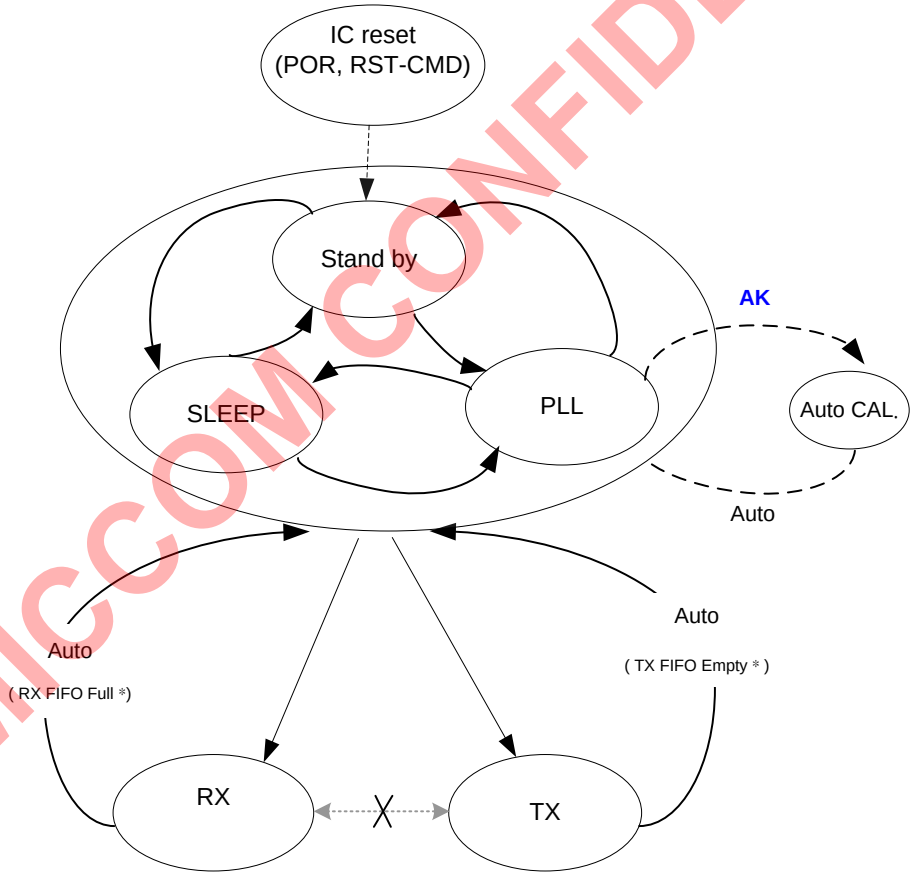


Figure 11.1 State machine

11.1 Key states

After power on reset or software reset, user has to do calibration process because all control registers are in initial values. The calibration process of A5133 is very easy, user only needs to issue Strobe commands and enable calibration registers. And then, the calibrations are automatically completed by A5133's internal state machine. Table 11.1 shows a summary of key circuitry among those strobe commands.

Strobe Command when AFIDS =0 (3Eh) and MIDS =0 (3Eh)

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	x	x	x	x	Sleep mode
1	0	0	1	x	x	x	x	Idle mode
1	0	1	0	x	x	x	x	Standby mode
1	0	1	1	x	x	x	x	PLL mode
1	1	0	0	x	x	x	x	RX mode
1	1	0	1	x	x	x	x	TX mode
1	1	1	0	x	x	x	x	FIFO write pointer reset
1	1	1	1	x	x	x	x	FIFO read pointer reset

Mode	Register retention	Regulator		Xtal Osc.	VCO	PLL	RX	TX	Strobe Command
		VDD_D	VDD_A(VDD_P)						
Sleep	Yes	ON	OFF	OFF	OFF	OFF	OFF	OFF	(1000-xxxx)b
Idle	Yes	ON	ON	OFF	OFF	OFF	OFF	OFF	(1001-xxxx)b
Standby	Yes	ON	ON	ON	OFF	OFF	OFF	OFF	(1010-xxxx)b
PLL	Yes	ON	ON	ON	ON	ON	OFF	OFF	(1011-xxxx)b
TX	Yes	ON	ON	ON	ON	ON	OFF	ON	(1101-xxxx)b
RX	Yes	ON	ON	ON	ON	ON	ON	OFF	(1100-xxxx)b

Remark: x means "don't care"

Table 11.1. Operation mode and strobe command

11.2 FIFO mode

This mode is suitable for the requirements of general purpose applications and can be chosen by setting FMS = 1. After calibration, user can issue Strobe command to enter standby mode where write TX FIFO or read RX FIFO. From standby mode to packet data transmission, only one Strobe command is needed. Once transmission is done, A5133 is auto back to standby mode. Figure 11.2 and Figure 11.3 are TX and RX timing diagram respectively. Time from T0 to T1 is about 120us (60us + 60us).

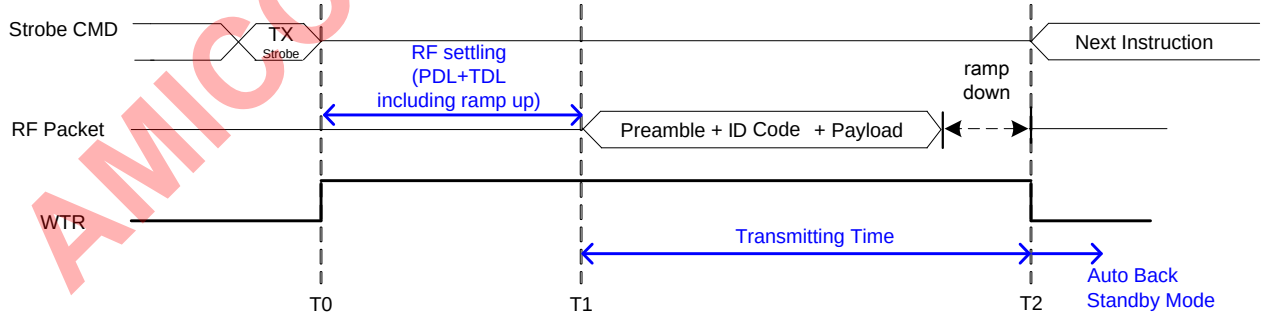


Figure 11.2 TX timing of FIFO Mode

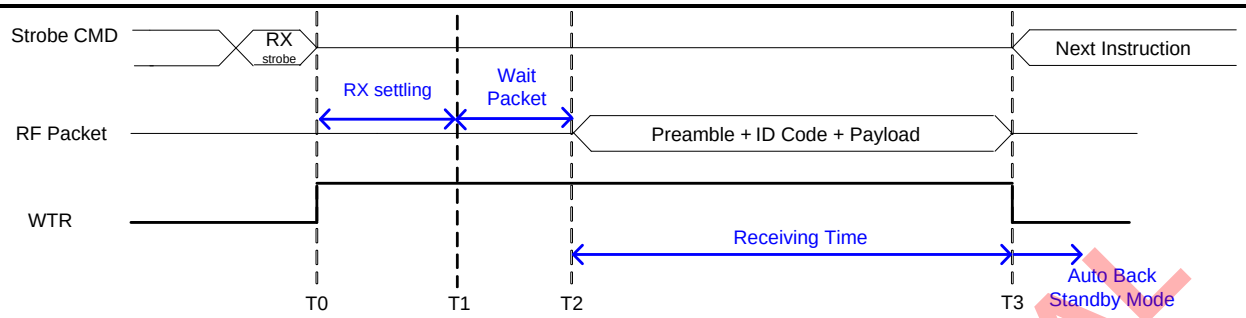


Figure 11.3 RX timing of FIFO Mode

11.3 Direct mode

This mode is suitable to let MCU to drive customized packet to A5133 directly by setting FMS = 0. In TX mode, MCU shall send customized packet in bit sequence (simply called raw TXD) to GIO1 or GIO2 pin. In RX mode, the receiving raw bit streams (simply called RXD) can be configured output to GIO1 or GIO2 pin. Be aware that a customized packet shall be preceded by a 32 bits carrier or preamble to let A5133 get a suitable DC estimation voltage. After calibration flow, for every state transition, user has to issue Strobe command to A5133 for fully manual control. This mode is also suitable for the requirement of versatile packet format. Figure 11.4 and Figure 11.5 are TX and RX timing diagram in direct mode respectively. Time from T0 to T1 is about 120us (60us + 60us).

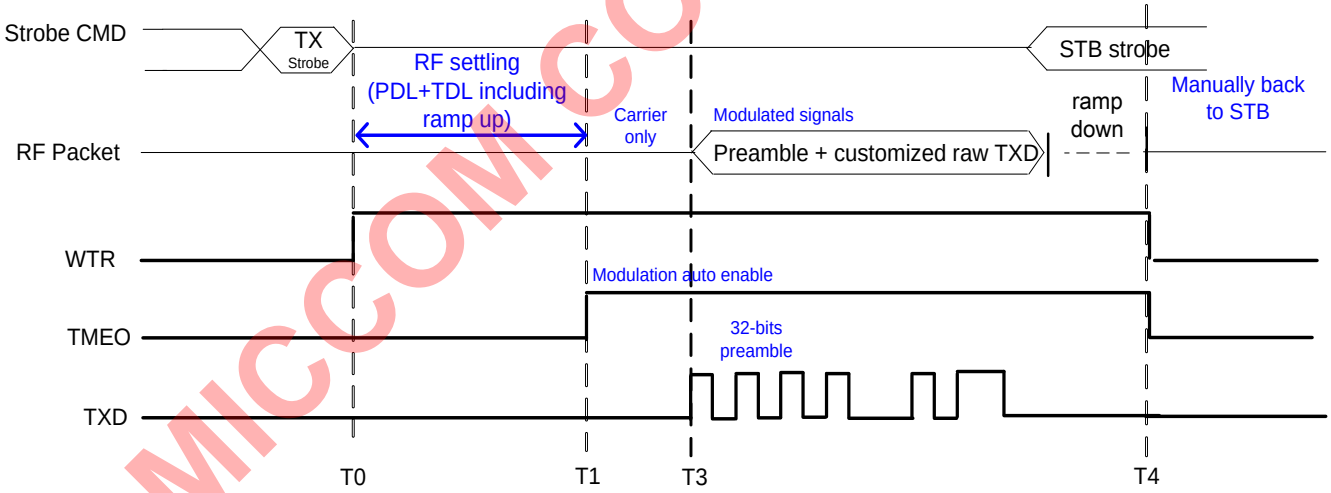


Figure 11.4 TX timing of Direct Mode

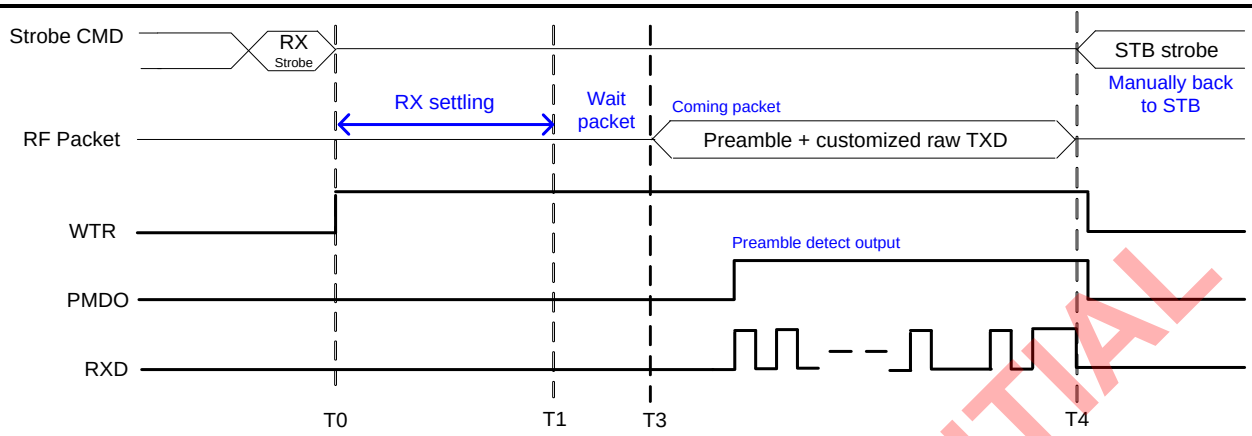


Figure 11.5 RX timing of Direct Mode

12. Crystal Oscillator

A5133 needs external crystal or external clock that is either 16 MHz to generate internal wanted clock.

Relative Control Register

Clock Register (Address: 0Dh)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	CGC1	CGC0	GRC3	GRC2	GRC1	GRC0	CGS	XS
R	IFS1	IFS0	GRC3	GRC2	GRC1	GRC0	--	--
Reset								

12.1 Use External Crystal

Figure 12.1 shows the connection of crystal network between XI and XO pins. C1 and C2 capacitance built inside A5133 are used to adjust different crystal loading. User can set CSXTL [7:0] to meet crystal loading requirement. A5133 supports low cost crystal within ± 35 ppm accuracy. Be aware that crystal accuracy requirement includes initial tolerance, temperature drift, aging and crystal loading.

Crystal Accuracy	Crystal ESR
±35 ppm	≦40 ohm

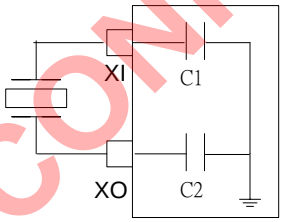


Figure 12.1 Crystal oscillator circuit, set CSXTL [7:0] for the internal C1 and C2 values.

12.2 Use External Clock

A5133 has built-in AC couple capacitor to support external clock input. Figure 11.2 shows how to connect. XS shall be low to select external clock. XCP and CSXTL are recommended to set to 0. The frequency accuracy of external clock shall be controlled within ± 35ppm, and the amplitude of external clock shall be within 0.8 ~ 1.2 V peak-to-peak.

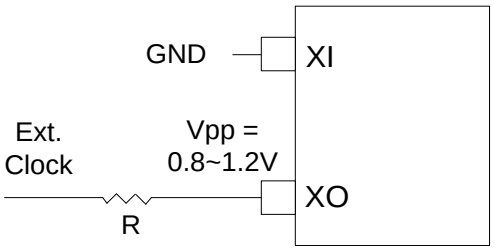


Figure 12.2 External clock source. R is used to tune Vpp = 0.8~1.2V

13. System Clock

A5133 supports different crystal frequency by programmable “Clock Register”. Based on this, three important internal clocks F_{CGR}, F_{DR} and F_{MSYCK} are generated.

(1) F_{XTAL}: Crystal frequency.
(2) F_{XREF}: Crystal Ref. Clock = F_{XTAL}
(3) F_{CGR}: Clock Generation Reference = 2MHz = F_{XREF} / (GRC+1).
(4) F_{IF}: Intermediate Frequency.
(5) F_{MSYCK}: Clock generator frequency= 16 * F_{IF} so that F_{MSYCK} depends on data rate.
(6) F_{DR}: Data Rate Clock = F_{IF} / (SDR+1).

Data Rate	F_{CGR}	F_{MSYCK}	F_{IF}	F_{DR}
4Mbps	2MHz	64MHz	4MHz	4MHz
2Mbps	2MHz	32MHz	2MHz	2MHz

Table 13.1 System clock and related clock sources

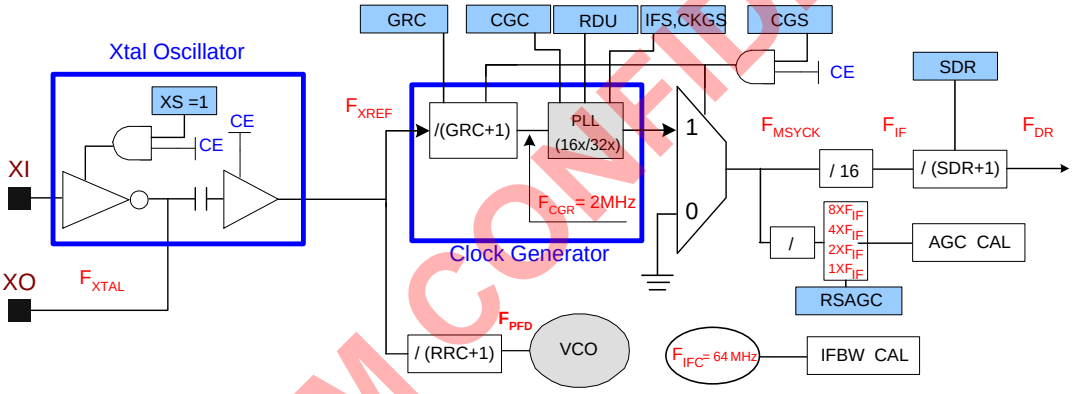


Figure 13.1 Block diagram of system clock and data rate clock

13.1 Data Rate Setting (4Mbps)

User can choose 16MHz XTAL for 4Mbps applications. The configurations of system clock is shown in Figure 13.2 and table 13.2.

Xtal	XS (0Dh)	GRC (0Dh)	CGC (0Dh)	RDU (1Ch)	CGS (0Dh)	SDR [7:0] (39h)	IFS [1:0] (1Ch)	CKGS [1:0](23h)	RSAGC [1:0] (1Bh)
16MHz	1	0111	00	0	1	0x00	11		11

Table 13.2 Registers configuration for 4Mbps.

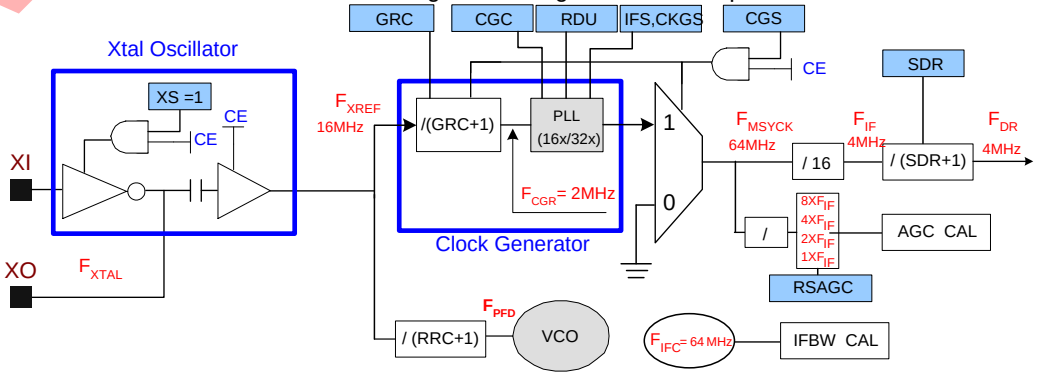


Figure 13.2 System clock and data rate clock for 4Mbps.

13.2 Data Rate Setting (2Mbps)

User can choose 16MHz XTAL for 2Mbps applications. The configurations of system clock is shown in Figure 13.3 and table 13.3.

Xtal	XS (0Dh)	GRC (0Dh)	CGC (0Dh)	RDU (1Ch)	CGS (0Dh)	SDR [7:0] (39h)	IFS [1:0] (1Ch)	CKGS [1:0](23h)	RSAGC [1:0] (1Bh)
16MHz	1	0111	00	0	1	0x00	01		11

Table 13.3 Registers configuration for 2Mbps.

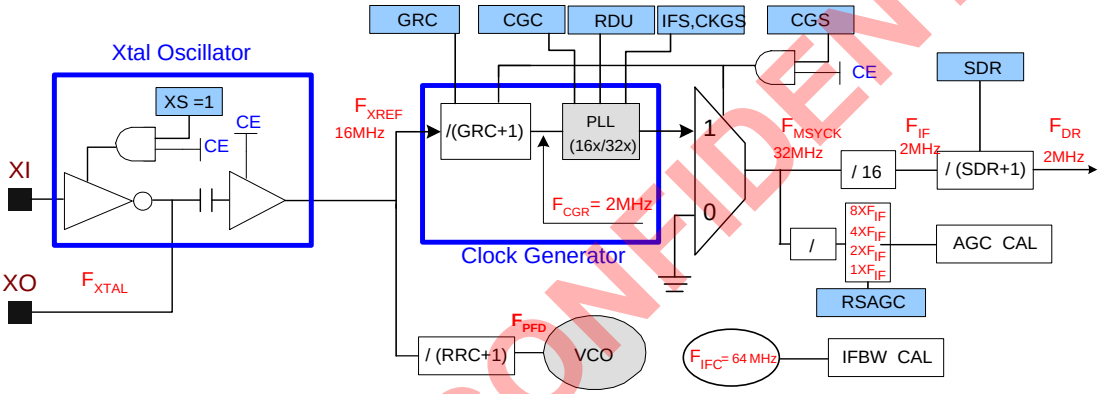


Figure 13.3 System clock and data rate clock for 2Mbps.

14. Transceiver LO Frequency

A5133 is a half-duplex low-IF transceiver with embedded PA and LNA. For TX or RX frequency setting, user just needs to set up RF frequency for two ways radio transmission.

To target full range of 5.8GHz band, A5133 applies offset concept by RF frequency $F_{RF} = F_{RF\_BASE} + F_{OFFSET.}$ Therefore, this device is easy to implement frequency hopping and multi-channels by just ONE register setting, PLL Register I (CHN [7:0]).

14.1 LO Frequency Setting

RF frequency F_{RF} in MHz is given directly by:
$F_{RF} = F_{RF\_BASE} + F_{OFFSET.}$
Where F_{RF_BASE} = 5725.001MHz
Where $F_{OFFSET.}$= CHN[7:0]*1MHz

For example: Set CHN[7:0]=100,
RF frequency(**F_{RF}**) = 5725.001MHz + (100 * 1MHz) = 5825.001MHz

15. Calibration

A5133 needs calibration process after power on reset or software reset. Below are six calibration items inside the device.

1. VCO Current Calibration.
2. VCO Bank Calibration.
3. VCO Deviation Calibration.
4. IF Filter Bank Calibration.
5. RC Oscillator Calibration.

15.1 Calibration Procedure

The purpose to execute the above calibration items is to deal with Foundry process deviation. After calibrations, A5133 will be set to the best working conditions without concerning Foundry process deviation to impact A5133's RF performance.

In general, user can use A5133's auto calibration function by just enabling calibration items and checking its calibration flag. For detailed calibration procedures, please refer to A5133 reference code of initRF() subroutine and A5133_Cal() subroutine.

1. Initialize A5133 by calling the subroutine of initRF().
   Initialize all control registers by calling the subroutine of A5133_Config().
   Execute all calibration items by calling the subroutine of A5133_Cal().

16. FIFO (First In First Out)

A5133 has the separated physical 64-bytes TX and RX FIFO inside the device. To use A5133's FIFO mode, user just needs to enable FMS =1. For FIFO accessing, TX FIFO (write-only) and RX FIFO (read-only) share the same register address 05h. TX FIFO represents transmitted payload. On the other hand, RX circuitry synchronizes ID Code and stores received payload into RX FIFO.

16.1 TX Packet Format in FIFO mode

16.1.1 Basic FIFO mode

A5133 has various parameters to select TX packet. Set CDPS=1(register 0x38, Page 5) to output preamble to replace carrier signal. Set EPML =0(20h, page 0) to no extend preamble output. Set IDL=[11] (20h, page 0) to use 8-byte ID length, The first 4-byte ID code is called SID1 and the second ID code is called SID2.If FCL[1:0] = 00 and EDRL = 0, A5133 is formed a Basic FIFO mode which can also support auto-ack/ auto-resend scheme. There is no MAC header in TX packet format. ID code is a PHY header used to be the frame sync to enable RX FIFO receiving.

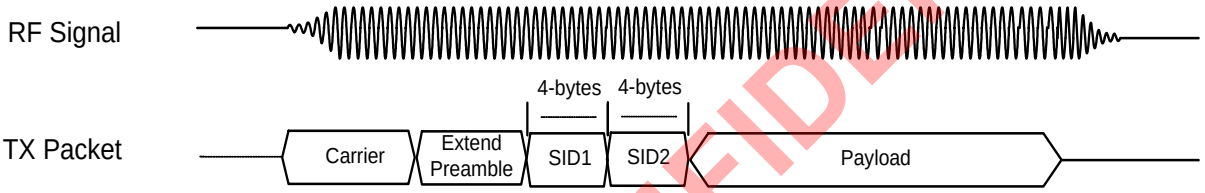


Figure 16.1TX packet with RF signal

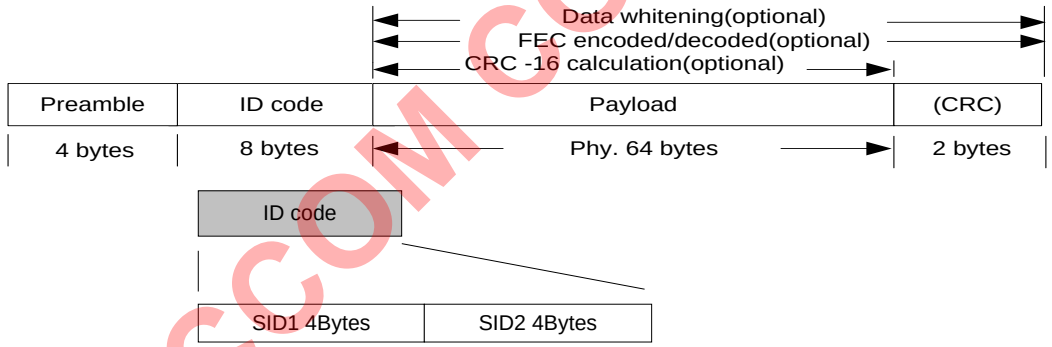


Figure 16.2 TX packet format of basic FIFO mode

Preamble:
Preamble is generated by CDPS in carrier signal interval. The sequence is fixed and the format is 0101…Use preamble to replace carrier signal by Set CDPS=1(register 0x38, Page 5).
The extend preamble is a self-generated preamble which is composed of alternate 0 and 1. If the first bit of ID code is 0, preamble shall be 0101…0101. In the contrast, if the first bit of SID code is 1, extend preamble shall be 1010…1010.
Extend preamble length is recommended to set 0 bytes by EPML [1:0] (20h, page 0).

ID code:
ID code is recommended to set 4 bytes by IDL[1:0] = [01] and ID Code is stored into ID Data register by sequence ID Byte 0, 1, 2 and 3. If RX circuitry check ID code is correct, payload will be written into RX FIFO. In addition, user can set ID code error tolerance (0~ 7bit error) by setting PTH [2:0] during ID synchronization check.

Payload:

Payload length is programmable by FEP. The physical FIFO depth is 64 bytes. A5133 supports logical FIFO extension to 4K bytes.

CRC:
In FIFO mode, if CRC is enabled (CRCS=1), 2-bytes of CRC value is self-generated and attached at the footer of the packet. In the same way, RX circuitry will check CRC value and show the result to CRC Flag.

16.1.2 Advanced FIFO mode

A5133 supports to self generated MAC header to form an advanced FIFO mode by enabling FCL[1:0], EDRL.. Therefore, A5133 can support ACK FIFO (FCB1~FCB3) and dynamic FIFO length depending on configurations.

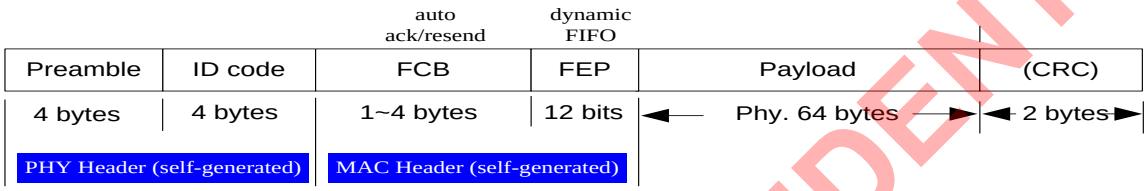


Figure 16.3 TX packet format of advanced FIFO mode.

FCB:
If FCL[1:0] ≠00, FCB header is enabled to support ACK FIFO by (FCB1~FCB3). The FCB is frame control byte. FCB0 is NOT allowed to program but carry a dedicated header (00111b) and TXSN [2:0] (Serial ID of packet number). FCB1~3 are used for customized information in FCB field.

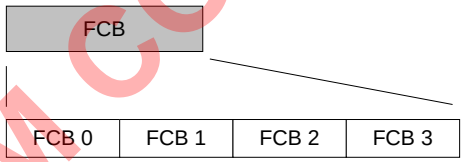


Figure 16.4 FCB (Frame Control Field)

FEP:
If EDRL = 1, A5133 supports dynamic FIFO. FEP [11:0] is self-generated to add into TX packet. In RX side, FEP[11:0] of the coming TX packet will be detected and stored into LENF [11:0] register.

HEC:
If HECS = 1, A5133 supports to self-generated a HEC byte which is a local CRC-8 of the MAC header. This HEC byte is an optional feature to calculate CRC result of MAC Header. HEC is located at the end of the MAC header.

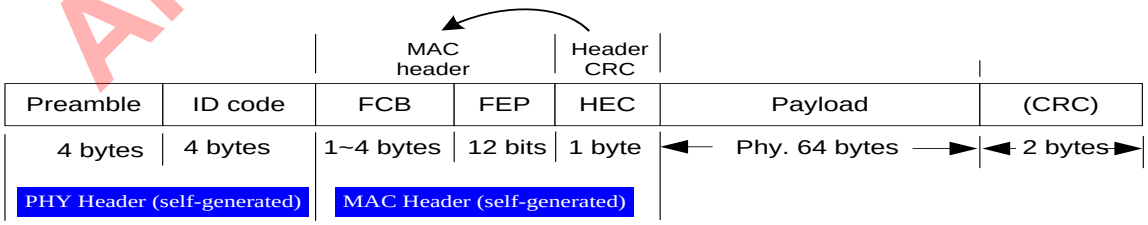


Figure 16.5 HEC (MAC header CRC)

16.2 Bit Stream Process in FIFO mode

A5133 supports 3 optional bit stream process for payload in FIFO mode, they are,

(1) CCITT-16 CRC
(2) (7, 4) Hamming FEC
(3) Data Whitening by XOR PN7 (7-bits Pseudo Random Sequence). The initial seed of PN7 is set by WS [6:0]

CRC (Cyclic Redundancy Check):

1. CRC is enabled by CRCS= 1. TX circuitry calculates the CRC value of payload (preamble and ID code are excluded) and transmits 2-bytes CRC value after payload.
2. RX circuitry checks CRC value and shows the result to CRCF. If CRCF=0, received payload is correct, else error occurred.

FEC (Forward Error Correction):

1. FEC is enabled by FECS= 1. Payload and CRC value (if CRCS=1) are encoded by (7, 4) Hamming code.
2. Each 4-bits (nibble) of payload is encoded into 7-bits code word and delivered out automatically.
   (ex., 64 bytes payload will be encoded to 128 code words, each code word is 7 bits.)
3. RX circuitry decodes received code words automatically. Each code word can correct 1-bit error. Once 1-bit error occurred, FECF=1 (00h).

Data Whitening:

1. Data whitening is enabled by WHTS= 1. Payload and CRC value (if CRCS=1) or their encoded code words (if FECS=1) are encrypted by bit XOR operation with PN7. The initial seed of PN7 is set by WS [6:0].
2. RX circuitry decrypts received payload and 2-bytes CRC (if CRCS=1) automatically. Please noted that user shall set the same WS [6:0] (22h) to TX and RX.

16.3 Transmission Time

Based on CRC and FEC options, the transmission time are different. See table 16.1 for details.

Data Rate = 4 Mbps

Data Rate (Mbps)	SID1 (bits)	SID2 Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
4	32	32	512	Disable	Disable	576 bit X 0.25 us = 144 us
4	32	32	512	16 bits	Disable	592 bit X 0.25 us = 148 us
4	32	32	512	Disable	512 x 7 / 4	960 bit X 0.25 us = 240 us
4	32	32	512	16 x 7 / 4	512 x 7 / 4	988 bit X 0.25 us = 247 us

Data Rate = 2 Mbps

Data Rate (Mbps)	SID1 (bits)	SID2 Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
2	32	32	512	Disable	Disable	576 bit X 0.5 us = 288 us
2	32	32	512	16 bits	Disable	592 bit X 0.5 us = 296 us
2	32	32	512	Disable	512 x 7 / 4	960 bit X 0.5 us = 480 us
2	32	32	512	16 x 7 / 4	512 x 7 / 4	988 bit X 0.5 us = 494 us

Table 16.1 Transmission time

16.4 Usage of TX and RX FIFO

In application points of view, A5133 supports 2 options of FIFO arrangement.
(1) Easy FIFO
(2) Segment FIFO

For FIFO operation, A5133 supports Strobe command to reset TX and RX FIFO pointer as shown below. User can refer to section 10.5 for details.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	1	0	x	x	X	x	FIFO write pointer reset (for TX FIFO)
1	1	1	1	x	x	X	x	FIFO read pointer reset (for RX FIFO)

16.4.1 Easy FIFO

In Easy FIFO mode, max FIFO length is 64 bytes. FIFO length is equal to **(FEP +1)**. User just needs to control FEP (03h) and disable PSA and FPM as shown below.

TX-FIFO (byte)	RX-FIFO (byte)	FEP[11:0] (03h)	PSA[5:0] (04h)	FPM[1:0] (04h)
1	1	0x00	0	0
8	8	0x07	0	0
16	16	0x0F	0	0
32	32	0x1F	0	0
64	64	0x3F	0	0

Table 16.2 Control registers of Easy FIFO

Procedures of TX FIFO Transmitting

1. Initialize all control registers (refer A5133 reference code).
2. Set FEP [11:0] = 0x003F for 64-bytes FIFO.
3. Send Strobe command – TX FIFO write pointer reset.
4. MCU writes 64-bytes data to TX FIFO.
5. Send TX Strobe Command and monitor WTR signal.
6. Done.

Procedures of RX FIFO Reading

1. When RX FIFO is full, WTR (or FSYNC) can be used to trigger MCU for RX FIFO reading.
2. Send Strobe command – RX FIFO read pointer reset.
3. MCU monitors WTR signal and then read 64-bytes from RX FIFO.
4. Done.

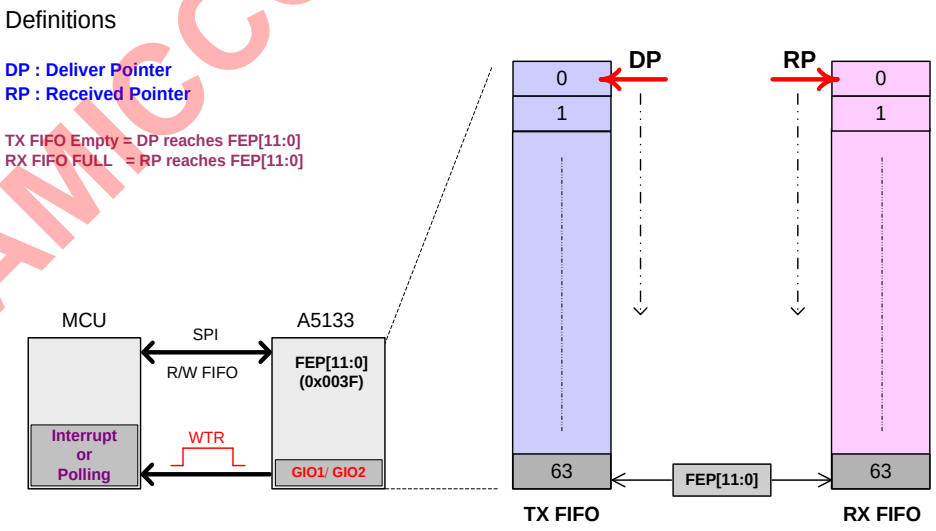


Figure 16.6 Easy FIFO

16.4.2 Segment FIFO

In Segment FIFO, TX FIFO length is equal to (FEP [11:0] – PSA [5:0]+1). FPM [1:0] should be zero. This function is very useful for button applications. In such case, each button is used to transmit fixed code (data) every time. During initialization, each fixed code is written into corresponding segment FIFO once and for all. Then, if button is triggered, MCU just assigns corresponding segment FIFO (PSA [5:0] and FEP [11:0]) and issues TX strobe command. Table 16.4 explains the details if TX FIFO is arranged into 8 segments, each TX segment and RX FIFO length are 8 bytes.

Segment	PSA	FEP	TX-FIFO (byte)	PSA[5:0] (04h)	FEP[11:0] (03h)	FPM[1:0] (04h)
1	PSA1	FEP1	8	0x00	0x07	0
2	PSA2	FEP2	8	0x08	0x0F	0
3	PSA3	FEP3	8	0x10	0x17	0
4	PSA4	FEP4	8	0x18	0x1F	0
5	PSA5	FEP5	8	0x20	0x27	0
6	PSA6	FEP6	8	0x28	0x2F	0
7	PSA7	FEP7	8	0x30	0x37	0
8	PSA8	FEP8	8	0x38	0x3F	0

RX-FIFO (byte)	PSA[5:0] (04h)	FEP[11:0] (03h)	FPM[1:0] (04h)
8	0	0x0007	0

Table 16.4 Segment FIFO is arranged into 8 segments

Procedures of TX FIFO Transmitting

1. Initialize all control registers (refer A5133 reference code).
2. Send Strobe command – TX FIFO write pointer reset.
3. MCU writes fixed code into corresponding segment FIFO once and for all.
4. To consign Segment 1, set PSA = 0x00 and FEP= 0x0007
   To consign Segment 2, set PSA = 0x08 and FEP= 0x000F
   To consign Segment 3, set PSA = 0x10 and FEP= 0x0017
   To consign Segment 4, set PSA = 0x18 and FEP= 0x001F
   To consign Segment 5, set PSA = 0x20 and FEP= 0x0027
   To consign Segment 6, set PSA = 0x28 and FEP= 0x002F
   To consign Segment 7, set PSA = 0x30 and FEP= 0x0037
   To consign Segment 8, set PSA = 0x38 and FEP= 0x003F
5. Send TX Strobe Command and monitor WTR signal.
6. Done.

Procedures of RX FIFO Reading

1. When RX FIFO is full, WTR (or FSYNC) is used to trigger MCU for RX FIFO reading.
2. Send Strobe command – RX FIFO read pointer reset.
3. MCU monitors WTR signal and then read 8-bytes from RX FIFO.
4. Done.

Definitions

DP : Deliver Pointer
RP : Received Pointer

TX FIFO Empty = DP reaches FEP[11:0]
RX FIFO FULL = RP reaches FEP[11:0]

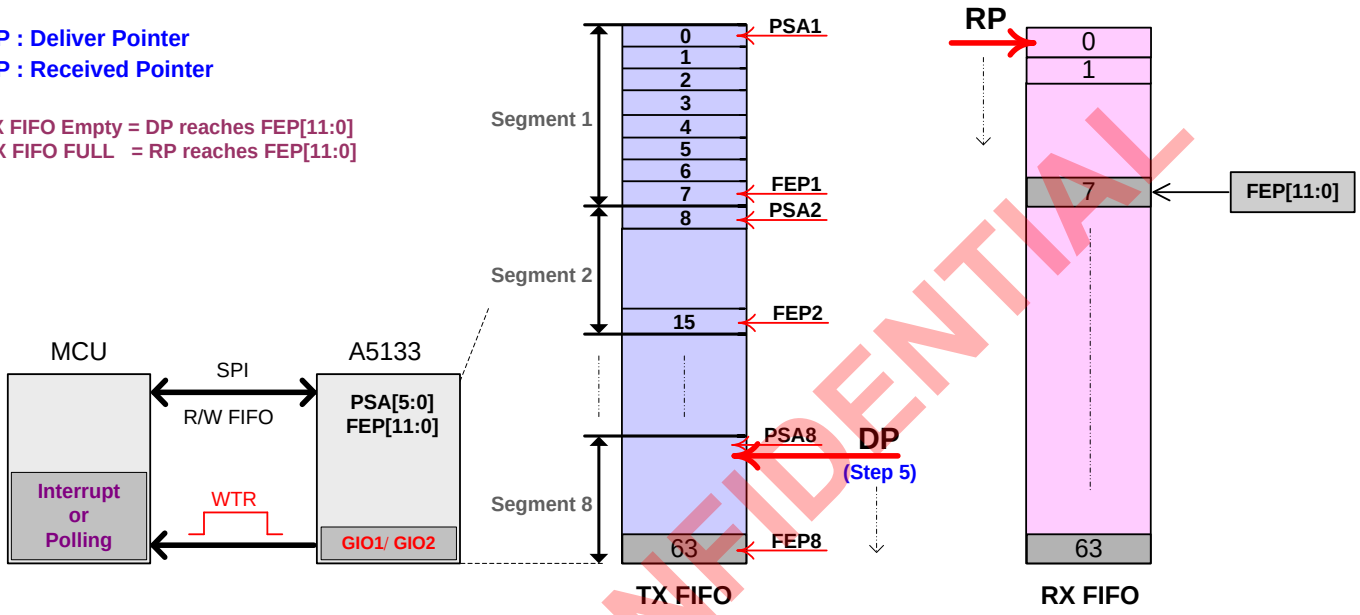


Figure 16.7 Segment FIFO Mode

17. ADC (Analog to Digital Converter)

A5133 has built-in 8-bits ADC for RSSI measurement and internal thermal sensor by enabling ADCM. User can just use the recommended values of ADC from Table 17.1. Please noted that ADC clock can be selected by setting FSARS (4MHz or 8MHz). The ADC converting time is 20 x ADC clock periods.

XADS (1Fh)	RSS (1Ch)	ARSSI (01h)	ADCM (01h)	ERSSM (1Ch)	FSARS (1Fh)	CDM (1Fh)	AVSEL [1:0] (1Fh)	Standby Mode	RX Mode
0	1	1	0	1	0	1	10	Thermal sensor	RSSI

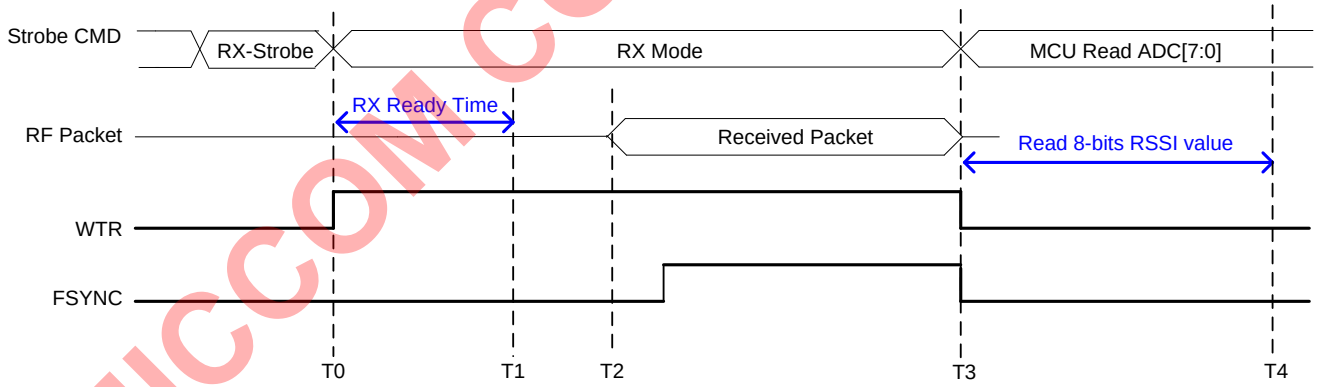
Table 17.1 Setting of RSSI measurement

17.1 RSSI Measurement

A5133 supports 8-bits digital RSSI to detect RF signal strength. RSSI value is stored in ADC [7:0] (1Eh). Be aware RSSI accuracy is about ± 6dB.

Auto RSSI measurement for TX Power of the coming packet:

1. Set wanted F_{RXLO}.
2. Set recommend values of Table 17.1.
3. Send RX Strobe command.
4. Once frame sync (FSYNC) is detected or exiting RX mode, user can read digital RSSI value from ADC [7:0] for TX power of the coming packet.

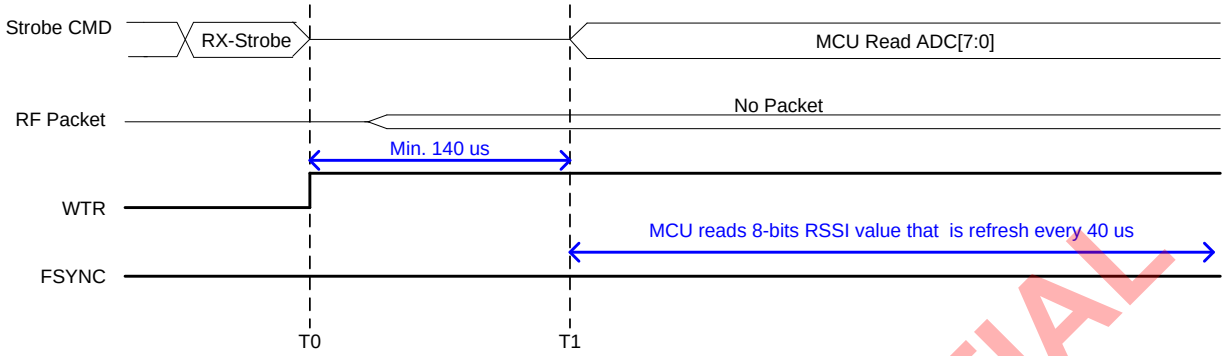


T0-T1: Settling Time
T2-T3: Receiving Packet
T3 : Exit RX mode automatically in FIFO mode
T3-T4: MCU read RSSI value @ ADC [7:0]

Figure 17.1 RSSI Measurement of TX Power of the coming packet.

Auto RSSI measurement for Background Power:

1. Set wanted F_{RXLO}.
2. Set recommend values of Table 17.1.
3. Send RX Strobe command.
4. Stay in RX mode at least 140 us and then exiting RX mode. User can read digital RSSI value from ADC [7:0] for the background power.



T0-T1: MCU Delay Loop from PLL to RX mode for RSSI measurment
T1 : Auto RSSI Measurment is done by 8-times average.
MCU can read RSSI value from ADC [7:0]

Figure 17.2 RSSI Measurement of Background Power.

18. Battery Detect

A5133 has a built-in battery detector to check supply voltage (REGI pin). The detecting range is 2.0V ~ 2.7V in 8 levels.

Battery detect Register (Address: 2Ch)

R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W	--	PM1S	BGS	QDS	BVT2	BVT1	BVT0	BD_E
R	--			BDF	BVT2	BVT1	BVT0	BD_E
Reset								

BDF : Low Battery Detection Flag.
[0]: battery low.
[1]: battery high.

BVT [2:0]: Battery Voltage Threshold Select.
[000]: 2.0V,
[001]: 2.1V.
[010]: 2.2V.
[011]: 2.3V.
[100]: 2.4V.
[101]: 2.5V.
[110]: 2.6V.
[111]: 2.7V.

BD_E: Battery Detect Enable.
[0]: Disable.
[1]: Enable.

Below is the procedure to detect low voltage input (ex. below 2.1V):

1. Set A5133 in standby or PLL mode.
2. Set BVT [2:0] = [001] and enable BD_E = 1.
3. After 5 us, user can read BDF or output BDF to GIO1 pin or CKO pin.
4. Set BD_E=0.

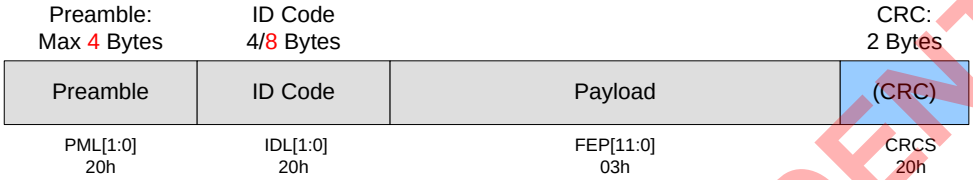
19. Auto-ack and auto-resend

A5133 supports auto-resend and auto-ack by setting EAK = 1 (auto-ack) and EAR = 1 (auto-resend). In application points of view, user may also enable auto-ack and auto-resend together with feature options of FCB and/or EDRL (dynamic FIFO).

19.1 Basic FIFO plus auto-ack auto-resend

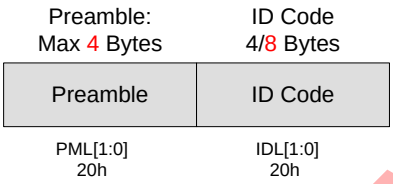
Set EAF = 0, EAK = 1 and EAR = 1 to enable auto-ack and auto-resend. Please refer to the below TX and ACK packet format of the sender and the receiver site respectively.

Sender Site (TX packet format)



The sender will repeat transmitting the above TX packet based on setting of ARC (3Ah) until the sender receives the below ACK packet successfully.

Receiver Site (ACK packet format)



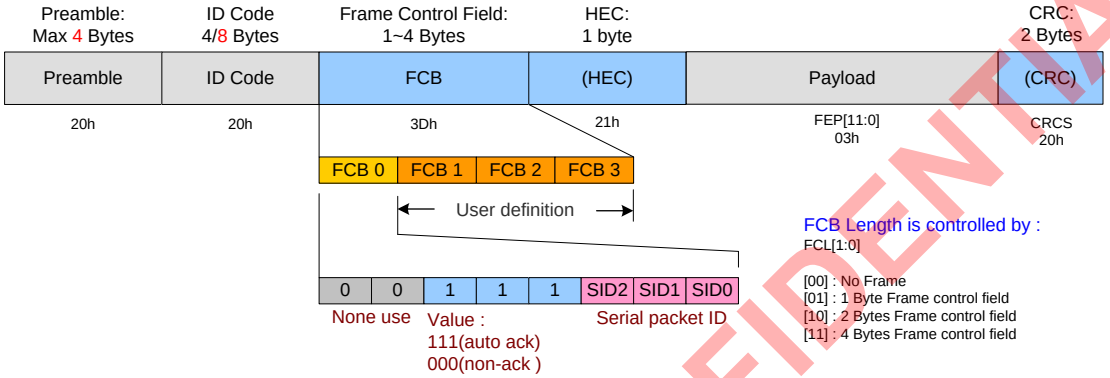
The receiver will automatically transmit the above ACK packet as long as the receiver gets the valid packet from the sender.

Figure 19.1 Sender site & Receiver site format of basic FIFO plus auto-ack auto-resend

19.2 Advanced FIFO plus auto-ack and auto-resend

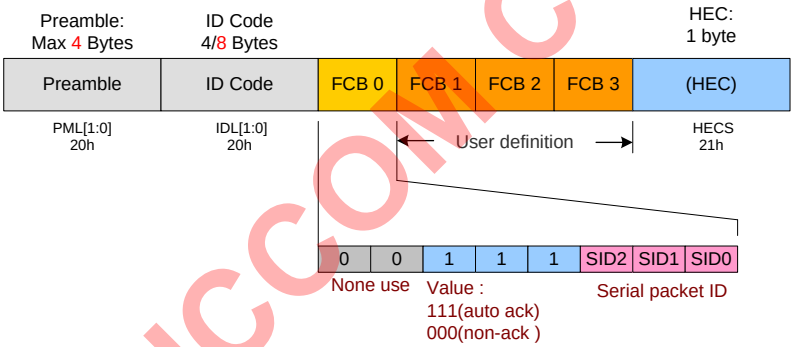
In addition to set EAF = 0, EAK = 1 and EAR = 1 to enable auto-ack and auto-resend. User can also enable an optional MAC header (FCB field) in the TX packet together with auto-ack and auto resend scheme. Please refer to the below TX and ACK packet format of the sender and the receiver site.

Sender Site (TX packet format)



The sender will repeat transmitting the above TX packet based on setting of ARC (3Ah) until the sender receives the below ACK packet successfully.

Receiver Site (ACK packet format)



The receiver will automatically transmit the above ACK packet as long as the receiver gets the above valid packet from the sender.

Figure 19.2 Sender site & Receiver site format of Advanced FIFO plus auto-ack auto-resend

19.3 WTR Behavior during auto-ack and auto-resend

If auto-ack and auto-resend are enabled (EAR = EAK = 1), WTR represents a completed transmission period and CWTR is a debug signal which represents the cyclic TX period and cyclic RX period. Please refer to the below timing diagrams for details.

The sender site (auto-resend)

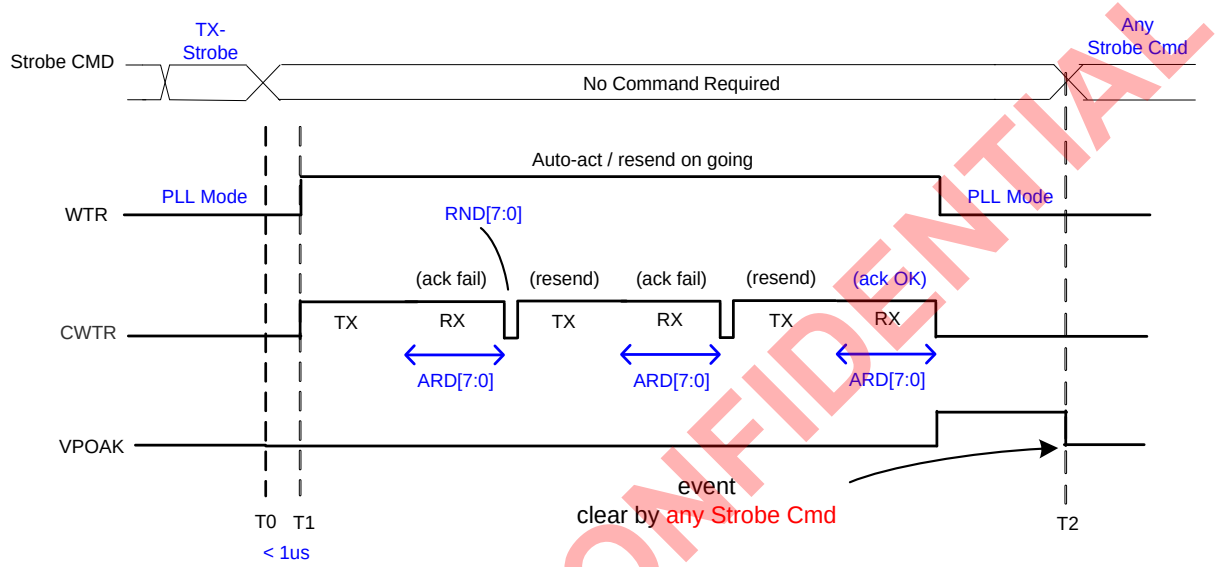
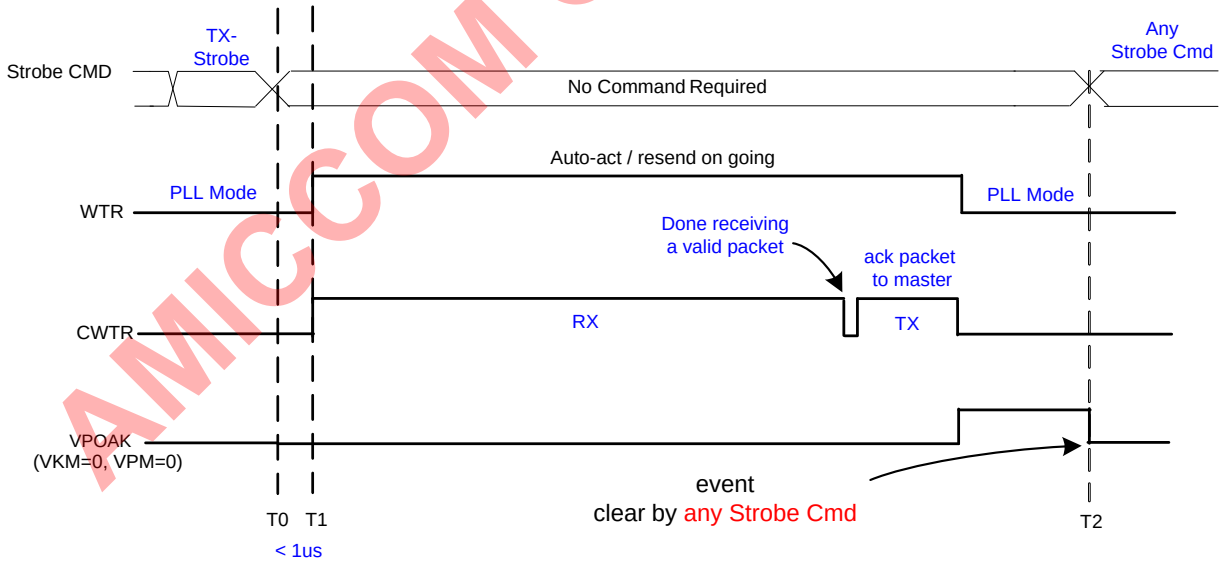


Figure 19.3 WTR Behavior timing of Sender site

The receiver site (auto-ack)



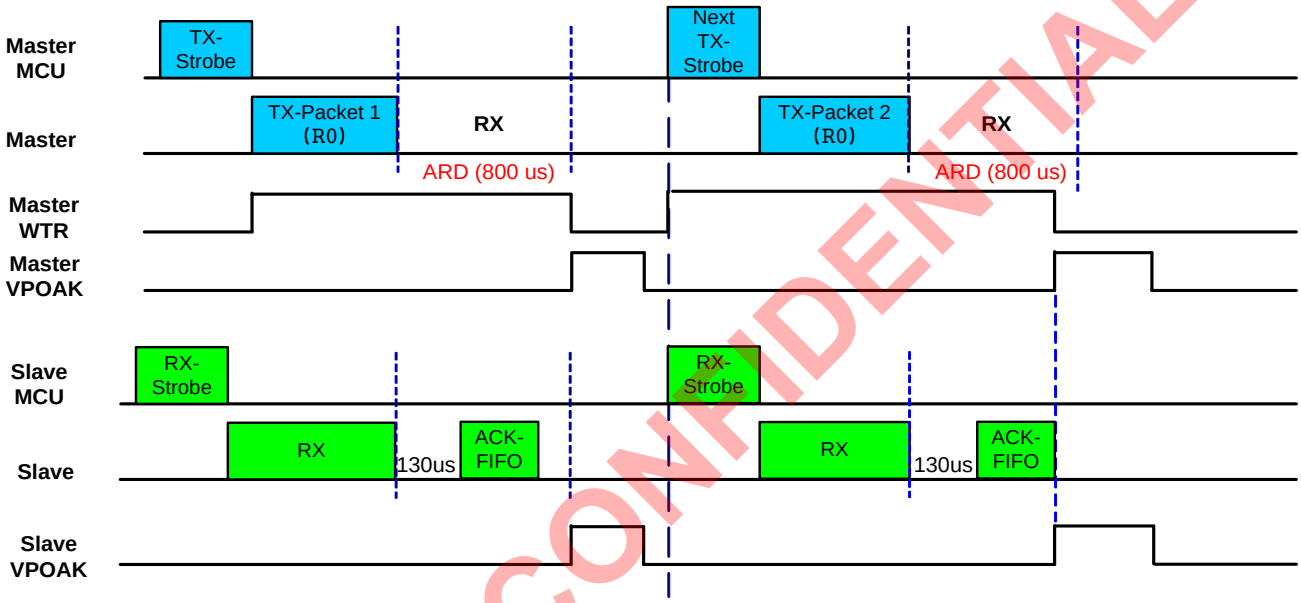
Remark: Refer to 3Bh for ARD[7:0] setting (auto resend delay).
Refer to 3Fh for RND[7:0] setting (random seed for resend interval).
Refer to 3Ah for EAK (enable auto-ack).
Refer to 3Ah for EAR (enable auto-resend).
Refer to 0Bh for VKM and VPM.

Figure 19.4 WTR Behavior timing of Receiver site

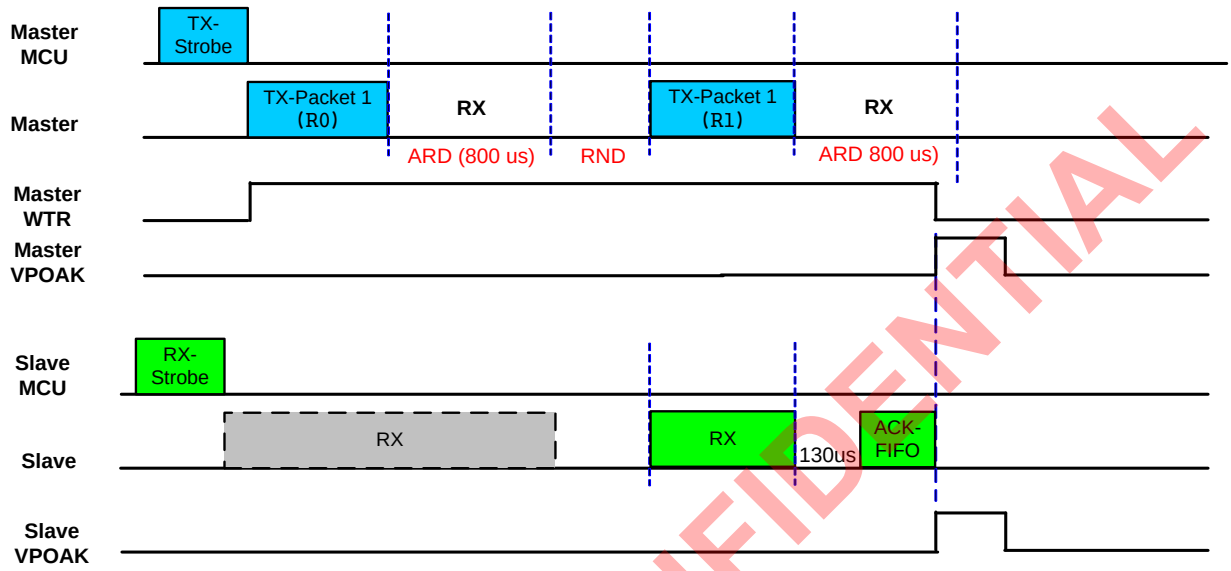
19.4 Examples of auto-ack and auto-resend

Once EAK and EAR are enabled, below case 1 ~ case 3 illustrate the most common cases as a timing reference (assume ARD = 800 us) in two ways radio communications.

<Case1> Always success



<Case2> Success in second packet



<Case3> always resend failure

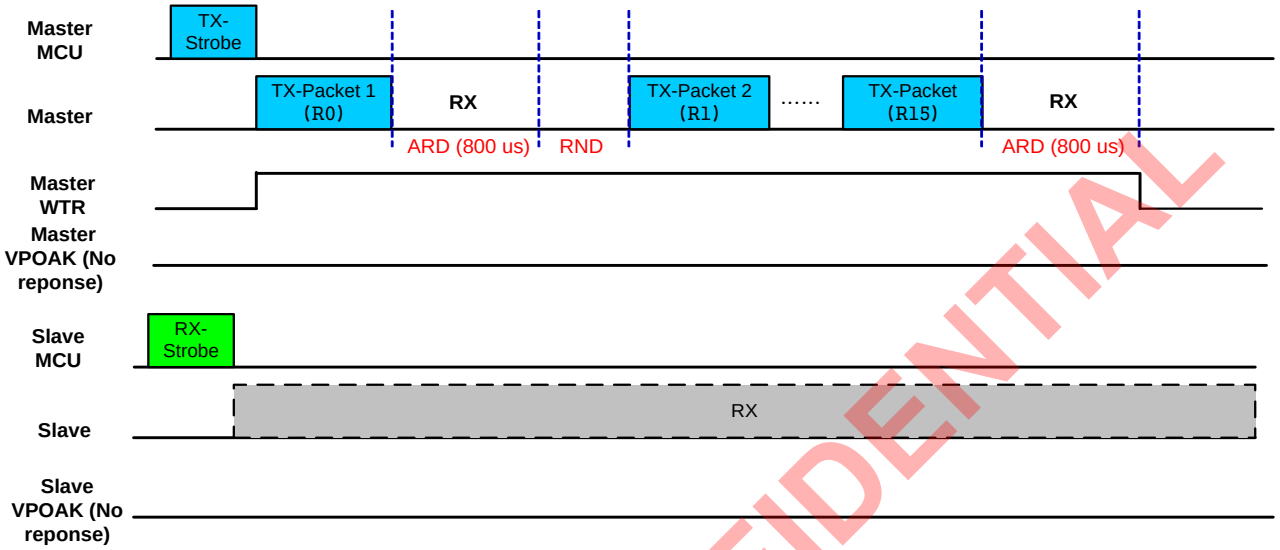


Figure 19.5 Examples timing of auto-ack and auto-resend

20. RC Oscillator

A5133 has an internal RC oscillator to supports TWOR (Timer Wake On) function. RCOSC_E (09h) is used to enable RC oscillator. TWOR_E (09h) is used to enable TWOR function. After done calibrations of RC oscillator, TWOR function can be operated from -40℃ to 85℃.

Parameter	Min	Typ	Max	Unit	Note
Calibrated Freq.	3.8K		4.2K	Hz	
Operation temperature	-40		85	℃	After calibration.

Table 20.1 basic characteristic of RC oscillator

20.1 WOR Function

When WOR is enabled (RCOSC_E=1, WORE=1 and TWOR_E=0), A5133 periodically wakes up from sleep and listen (auto-enter RX mode) for incoming packets without MCU interaction. Therefore, A5133 will stay in sleep mode based on WOR_SL timer and RX mode based on WOR_AC timer. After receiving a packet, A5133 will output TWOR (from either GIO1 or GIO2) to wake up MCU.
Meanwhile, A5133 will end WOR function and auto back to previous state.

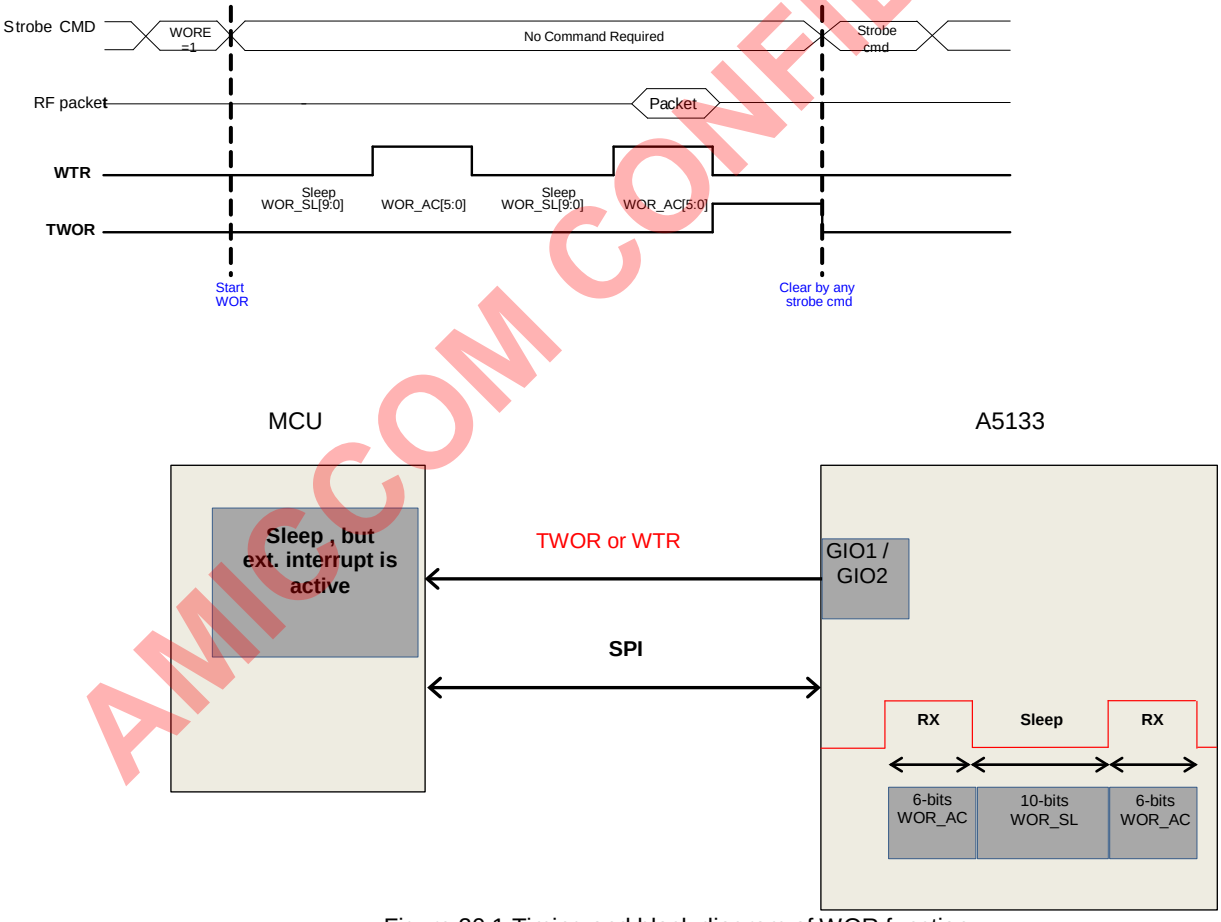


Figure 20.1 Timing and block diagram of WOR function

20.2 TWOR Function

The RC oscillator inside A5133 can also be used to supports programmable TWOR (Timer Wake-On, TWOR_E=1) function which enables A5133 to output a periodic square wave from GIO1 (or GIO2). The duty cycle of this square wave is set by WOR_AC (08h) or WOR_SL (08h and 07h) regarding to TSEL (09h). User can use this square wave to wake up MCU or other purposes.

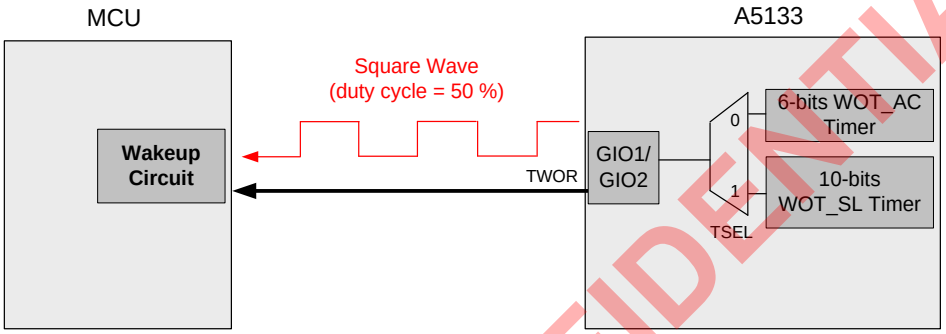


Figure 20.2 Block diagram of TWOR function

21. AES128 Security Packet

A5133 has a built-in AES128 security engine to generate a security packet by any general purpose MCU. In addition to support 128-bits key length (AES128), A5133 also support proprietary 32-bits key length called AES32.

Software procedure to use AES128.
Step1: Write 16-bytes AES128 key to KEYI [127:0] (36h)
Step2: Set AESS=1 (3Eh) to select standard AES128
Step3. Set AKFS=0 (3Eh) to not attach AES128 KEYI [127:0] to the wanted TX packet.
Step4: Set EDCRS=1 (3Eh) to enable AES128.
Step5: Write plain text to TX FIFO
Step6: Issue TX strobe command and then A5133 will execute AES128 encryption and deliver the cipher text without latency.
Step7: In RX side with the same configurations, A5133 will execute AES128 decryption and store plain text back to RX FIFO.

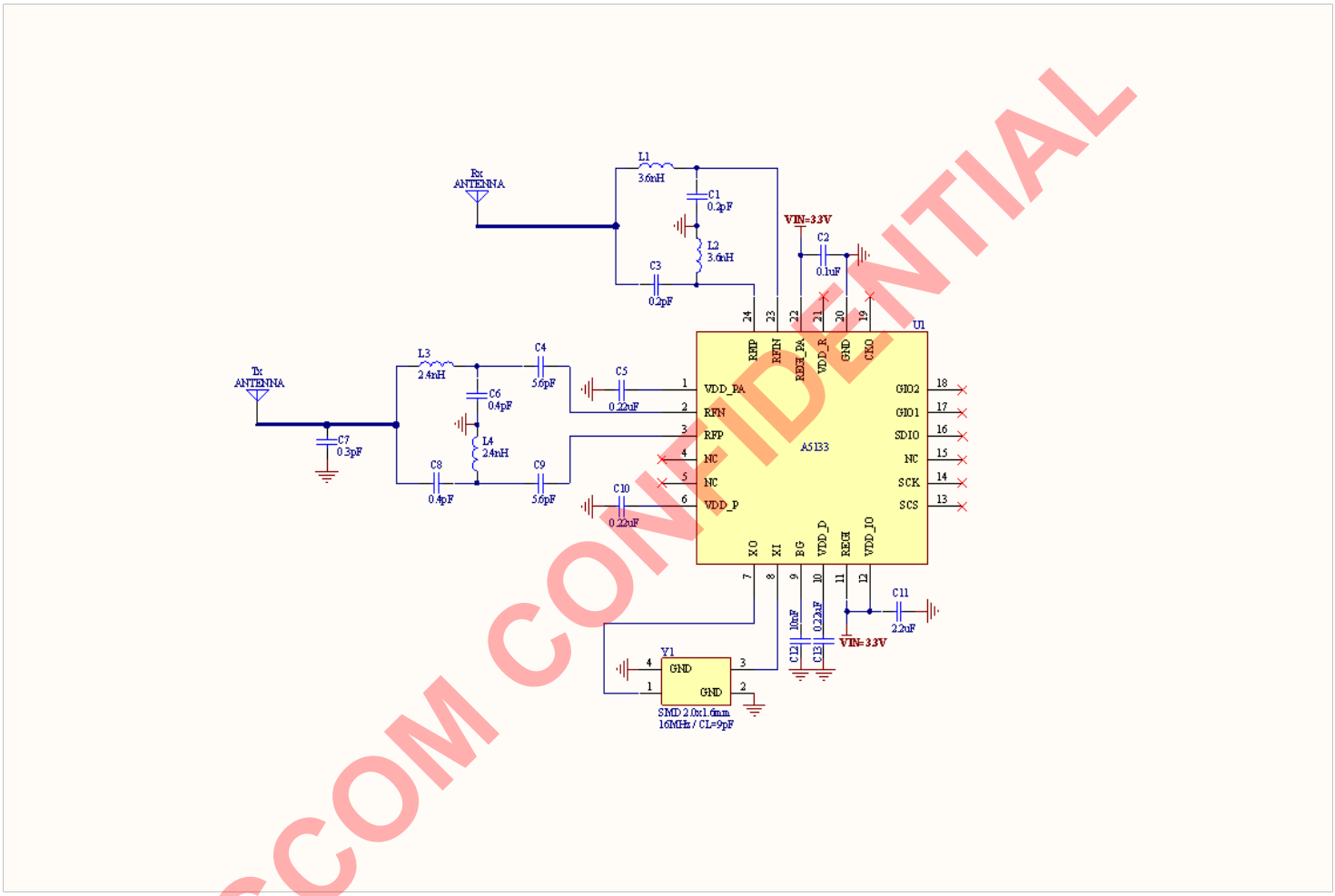
Remark
1. The unit size of AES128 encryption packet is 16-bytes.
2. In TX side, if plain text is not dividable by 16-bytes, i.e. 5-bytes only, the TX packet is complement to 16-bytes.
3. In RX side, the coming cipher text will be decrypted and restore 5-bytes plain text back to RX FIFO.

Software procedure to use AES32.
Step1: Write 4-bytes AES128 key to KEYI [31:0] (36h)
Step2: Set AESS=0 (3Eh) to select proprietary AES32.
Step3. Set AKFS=0 (3Eh) to not attach AES128 KEYI [31:0] to the wanted TX packet.
Step4: Set EDCRS=1 (3Eh) to enable AES128.
Step5: Write plain text to TX FIFO
Step6: Issue TX strobe command and then A5133 will execute AES32 encryption and deliver the cipher text without latency.
Step7: In RX side with the same configurations, A5133 will execute AES32 decryption and store plain text back to RX FIFO.

Remark
1. The unit size of AES32 encryption packet is 4-bytes.
2. In TX side, if plain text is not dividable by 4-bytes, i.e. 5-bytes only, the TX packet is complement to 8-bytes.
3. In RX side, the coming cipher text will be decrypted and restore 5-bytes plain text back to RX FIFO.

22. Application circuit

Below are AMICCOM's ref. design circuits. For more details, please contact AMICCOM's FAE for more details.



23. Abbreviations

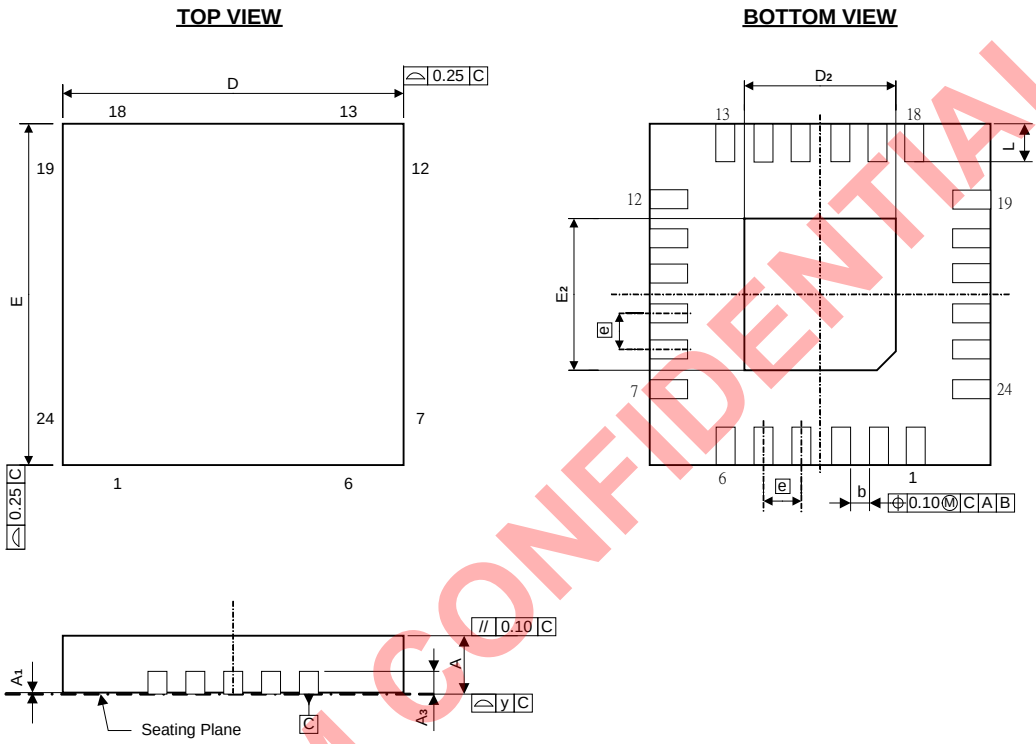
ADC	Analog to Digital Converter
AIF	Auto IF
FC	Frequency Compensation
AGC	Automatic Gain Control
BER	Bit Error Rate
BW	Bandwidth
CD	Carrier Detect
CHSP	Channel Step
CRC	Cyclic Redundancy Check
DC	Direct Current
FEC	Forward Error Correction
FIFO	First in First out
FSK	Frequency Shift Keying
ID	Identifier
IF	Intermediate Frequency
ISM	Industrial, Scientific and Medical
LO	Local Oscillator
MCU	Micro Controller Unit
PFD	Phase Frequency Detector for PLL
PLL	Phase Lock Loop
POR	Power on Reset
RX	Receiver
RXLO	Receiver Local Oscillator
RSSI	Received Signal Strength Indicator
SPI	Serial to Parallel Interface
SYCK	System Clock for digital circuit
TX	Transmitter
TXRF	Transmitter Radio Frequency
VCO	Voltage Controlled Oscillator
XOSC	Crystal Oscillator
XREF	Crystal Reference frequency
XTAL	Crystal

24. Ordering Information

Part No.	Package	Units Per Reel / Tray
A51U33AQCI/Q	QFN4x4, Pb Free, Tape & Reel, -40℃～85℃	3K
A51U33AQCI	QFN4x4, Pb Free, Tray, -40℃～85℃	490EA
A51U33AH	Die form, -40℃～85℃	100EA

25. Package Information

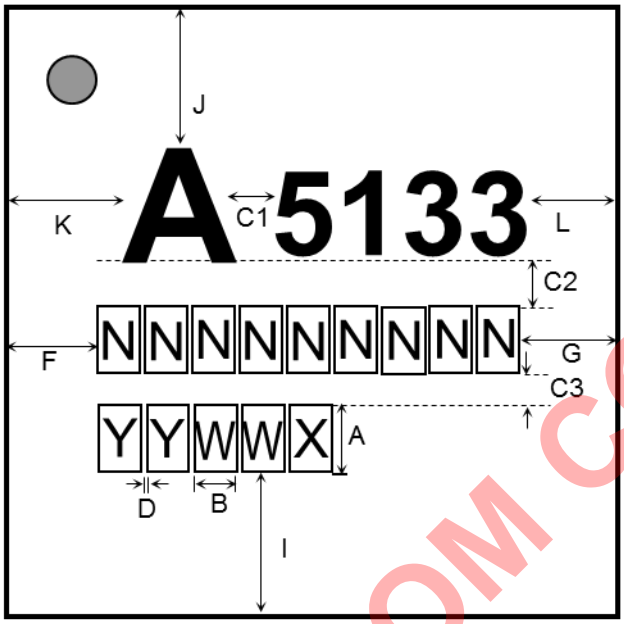
QFN4X4 24L Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.028	0.030	0.032	0.70	0.75	0.80
A_1	0.000	0.001	0.002	0.00	0.02	0.05
A_3		0.008 REF			0.203 REF	
b	0.007	0.010	0.012	0.18	0.25	0.30
D	0.154	0.158	0.161	3.90	4.00	4.10
D_2	0.075	0.104	0.114	1.90	2.65	2.90
E	0.154	0.158	0.161	3.90	4.00	4.10
E_2	0.075	0.104	0.114	1.90	2.65	2.90
e		0.020 BSC			0.50 BSC	
L	0.012	0.016	0.020	0.30	0.40	0.50
y		0.003			0.08	

26. Top Marking Information

- Part No. : **A51U33AQCI**
- Pin Count : **24**
- Package Type : **QFN 4x4**
- Dimension : **4*4 mm**
- Mark Method : **Laser Mark**
- Character Type : **Arial**



❖ **CHARACTER SIZE : (Unit in mm)**

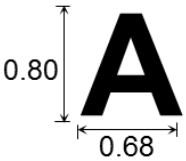
A : 0.55
B : 0.36
C1 : 0.25 C2 : 0.3 C3 : 0.2
D : 0.03

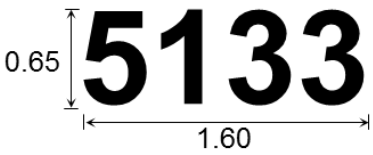
F=G
I=J
K=L

YYWW : DATECODE

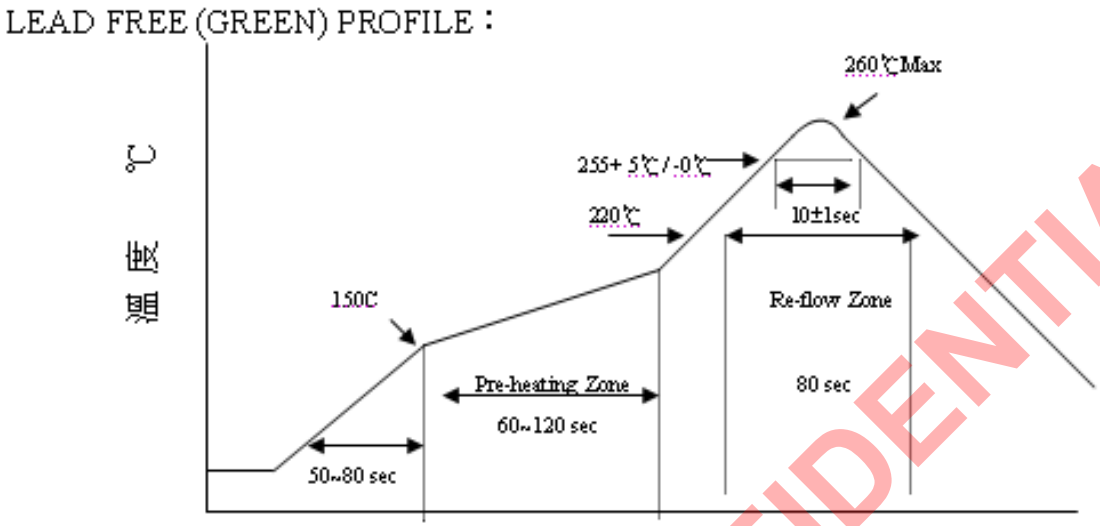
X : PKG HOUSE ID

NNNNNNNNN : LOT NO.
(max. 9 characters)





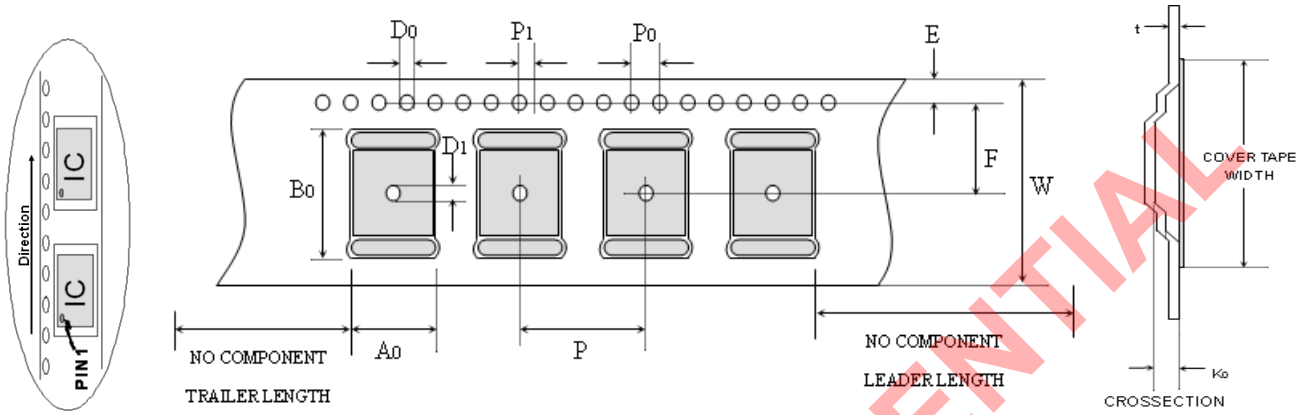
27. Reflow Profile



Actual Measurement Graph

28. Tape Reel Information

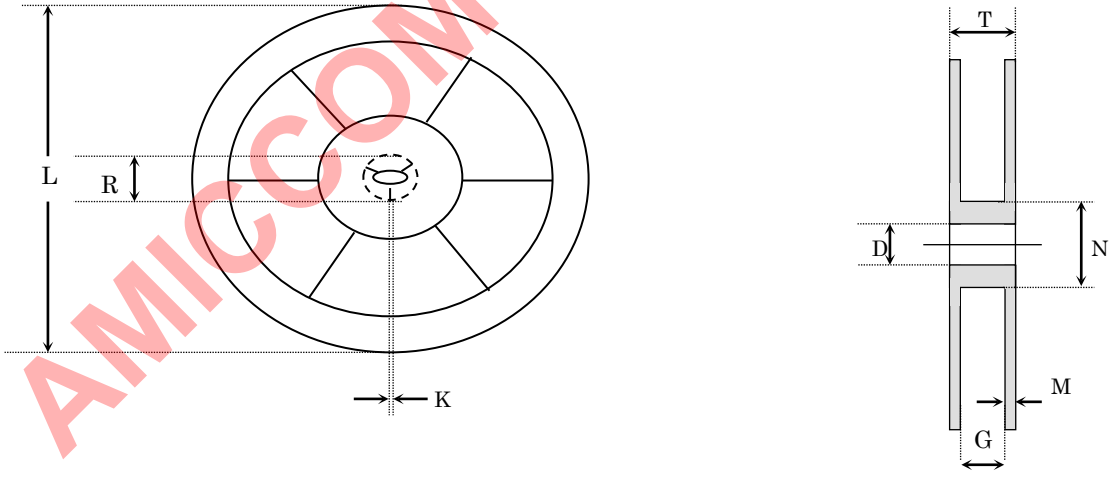
Cover / Carrier Tape Dimension



Unit: mm

TYPE	P	A0	B0	P0	P1	D0	D1	E	F	W	K0	t	Cover tape width
QFN3*3	8±0.1	3.2 5±0.1	3.25 ±0.1	4±0.2	2±0.1	1.5±0.1	1.5	1.75 ±0.1	5.5 ±0.05	12±0.3	1.25 ±0.1	0.3 ±0.05	9.3±0.1
QFN 4*4	8±0.1	4.35 ±0.1	4.35 ±0.1	4±0.2	2±0.1	1.5±0.1	1.5	1.75 ±0.1	5.5 ±0.05	12±0.3	1.2 5±0.1	0.3 ±0.05	9.3±0.1
QFN 5*5	8±0.1	5.25 ±0.1	5.25 ±0.1	4±0.2	2±0.1	1.5±0.1	1.5	1.75 ±0.1	5.5 ±0.05	12±0.3	1.25 ±0.1	0.3 ±0.05	9.3±0.1
SSOP	12±0.1	8.2±1	8.8±1.5	4.0±0.1	2.0±0.1	1.5±0.1	1.5±0.1	1.75 ±0.1	7.5±0.1	16±0.1	2.1±0.4	0.3 ±0.05	13.3 ±0.1

REEL DIMENSIONS



Unit: mm

TYPE	G	N	M	D	K	L	R
QFN	12.9±0.5	102 REF±2.0	2.3±0.2	13.15±0.35	2.0±0.5	330±3.0	19.6±2.9
SSOP	16.3±1	102 REF±2.0	2.3±0.2	13.15±0.35	2.0±0.5	330±3.0	19.6±2.9

29. Product Status

Data Sheet Identification	Product Status	Definition
Objective	Planned or Under Development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification	Noted Full Production	This data sheet contains the final specifications. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by AMICCOM. The data sheet is printed for reference information only.

Headquarte
10F., No.18, Taiyuan St., Zhubei City, Hsinchu County 30265, Taiwan, R.O.C.
Tel : 886-3-5601717

Web Site
http://www.amiccom.com.tw